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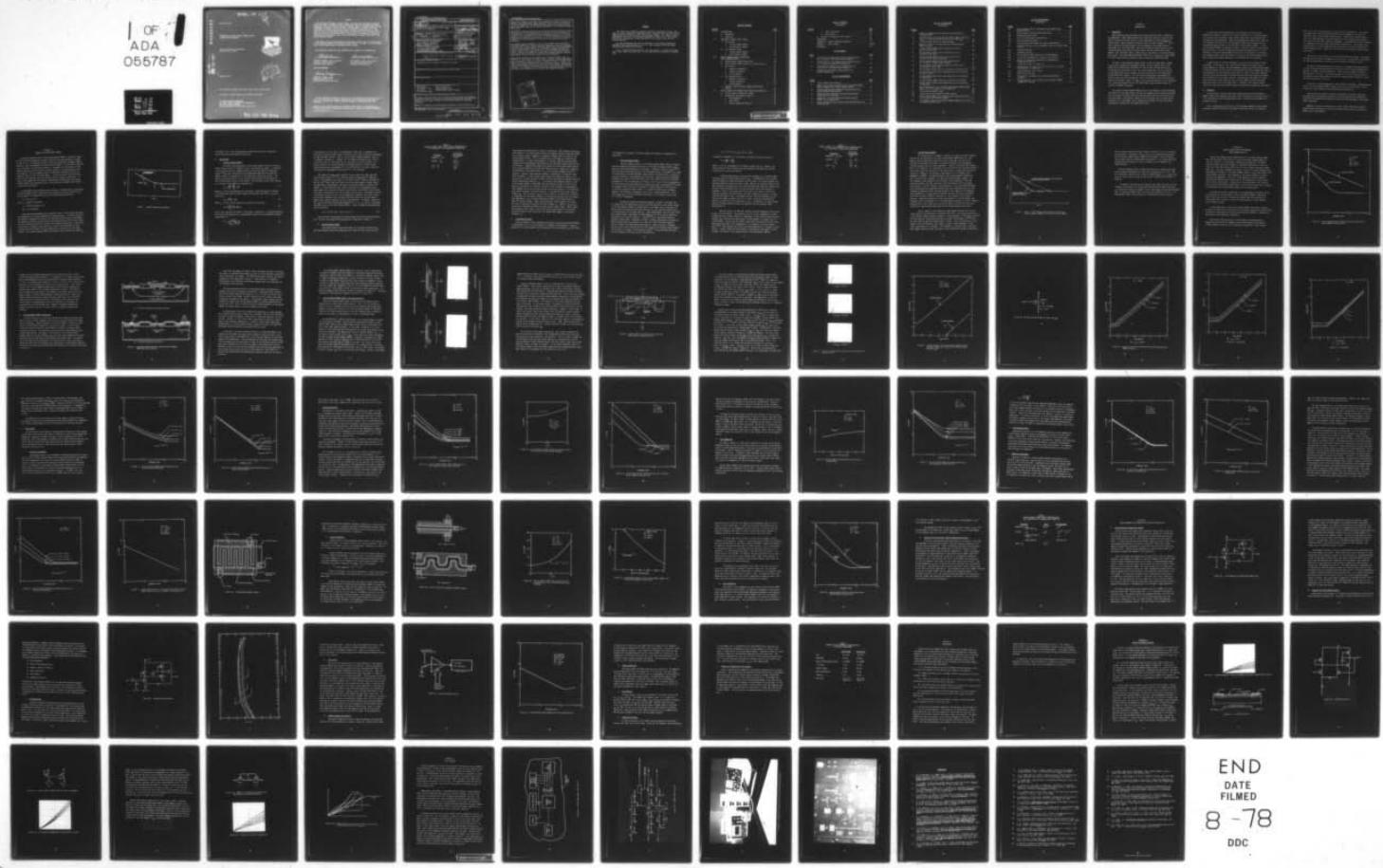
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INTEGRATED LOW NOISE BURIED CHANNEL MOSFET
PREAMPLIFIER TECHNOLOGY

Texas Instruments Incorporated
Dallas, Texas 75222



December 1977



Final Technical Report for period 1 April 1976 - 30 June 1977

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AIR FORCE AVIONICS LABORATORY
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This technical report has been reviewed and is approved for publication.

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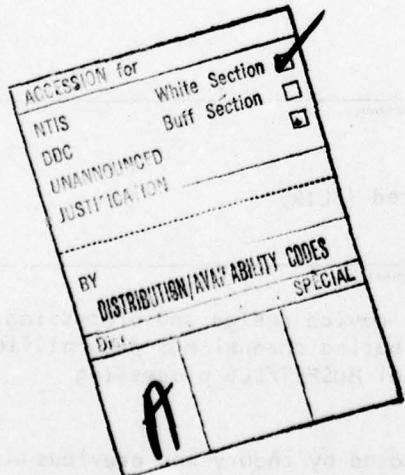
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experimental evidence to influence noise performance in MOSFET structures were defined. The buried channel MOSFET was chosen as the vehicle for achieving low level preamplifier noise characteristics because of its superior low frequency noise performance and its process-compatibility with the buried channel CCD process.

Experimental evaluation was carried out on existing devices processed at Texas Instruments prior to the beginning of this contract, and from the results of that evaluation a low noise buried channel MOS preamplifier bar was designed. In addition to the preamplifier circuit, the design included a matrix of test MOSFETs, both surface and buried channel, to allow a more extensive evaluation of MOSFET noise characteristics as a function of the previously mentioned parameters.

Low frequency noise performance in buried channel MOSFETs was discovered to be strongly dependent on several processing parameters, as well as on design parameters such as device geometry and bias. The strong functional dependence of low frequency excess noise in the buried channel structure on gate oxide thickness, gate material, and channel depth is not apparent from existing theory. However, the preamplifier input stages were designed with thin gate oxide, polysilicon gate material, and deep buried channel implants, based on experimental results indicating optimum low noise performance.

Experimental evaluation of the preamplifiers revealed the design goals are being met in terms of gain (37.2 dB), linearity (0.43%), dynamic range (80 dB), power dissipation (27 mW), and frequency response (60 kHz). The noise levels appear to be higher than expected in the low frequency region. However, the large interdigitated MOSFET test devices, which are also used as preamplifier input MOSFETs, exhibit low frequency noise levels much greater than predicted by theory. This suggests that the low frequency noise performance of the preamplifiers can be improved with a different input MOSFET architecture.



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PREFACE

This report was prepared by Texas Instruments Incorporated, Dallas, Texas under Air Force Contract No. F33615-76-C-1221. The work under this contract was administered and funded by the Air Force Systems Command. Mr. Robert M. Werner (AFAL/DHE-2) of the Air Force Avionics Laboratory, a part of Air Force Wright Aeronautical Laboratories, Wright-Patterson Air Force Base, Ohio, was the Project Engineer.

At Texas Instruments the work was performed in the Advanced Technology Laboratory under the direction of Dr. D. D. Buss, Manager of the CCD Signal Processing and Advanced FLIR branch.

This is the Final Technical Report for the contract. It covers work done from 1 April 1976 to 30 June 1977. It was submitted by the authors in December 1977.

TABLE OF CONTENTS

| <u>SECTION</u> | | <u>PAGE</u> |
|----------------|---|-------------|
| I | INTRODUCTION | 1 |
| | A. Background | 1 |
| | B. Objective | 2 |
| II | OVERVIEW OF MOSFET NOISE THEORY | 4 |
| | A. White Noise | 6 |
| | 1. Surface Channel MOSFET | 6 |
| | 2. Buried-Channel MOSFET | 7 |
| | B. Low Frequency Noise | 9 |
| | 1. Surface Channel MOSFET | 10 |
| | 2. Buried Channel MOSFET | 13 |
| III | BURIED CHANNEL MOSFET EXPERIMENTAL NOISE CHARACTERISTICS | 16 |
| | A. Buried Channel MOSFET Fabrication | 18 |
| | B. Buried Channel MOSFET Output I-V Characteristics | 21 |
| | C. White Noise | 32 |
| | 1. Geometric Parameters | 32 |
| | 2. Process Parameters | 35 |
| | 3. Bias Parameters | 39 |
| | D. Low Frequency Noise | 42 |
| | 1. Geometric Parameters | 42 |
| | 2. Process Parameters | 49 |
| | 3. Bias Parameters | 53 |
| | E. Summary of Buried Channel MOSFET Experimental Results | 55 |
| IV | BURIED CHANNEL MOS PREAMPLIFIER DESIGN AND EVALUATION | 57 |
| | A. Buried Channel Preamplifier Design | 57 |
| | B. Preamplifier Experimental Results | 59 |
| | 1. Gain/Bandwidth | 60 |
| | 2. Input Noise | 63 |
| | 3. Dynamic Range and Linearity | 63 |

TABLE OF CONTENTS
(continued)

| <u>SECTION</u> | | <u>PAGE</u> |
|----------------|---|-------------|
| | 4. Power Dissipation | 66 |
| | 5. Bias Effects | 66 |
| | C. Summary of Preamplifier Test Results | 67 |
| V | CONCLUSIONS | 69 |
| | APPENDIX A - LINEAR INTEGRATED RESISTOR. | 71 |
| | APPENDIX B - TEST FIXTURE. | 78-79 |
| | REFERENCES | 84 |

LIST OF TABLES

| <u>TABLE</u> | | <u>PAGE</u> |
|--------------|---|-------------|
| 1 | Surface Channel MOSFET White Noise Characteristics As a Function of the Generalized Parameters | 8 |
| 2 | Surface Channel Low Frequency Noise Characteristics as a Function of Generalized Parameters | 12 |
| 3 | Buried Channel MOSFET Noise Characteristics as a Function of the Generalized Parameters | 56 |
| 4 | Preamplifier Performance Characteristics at Ambient Temperature | 68 |

LIST OF ILLUSTRATIONS

| <u>FIGURE</u> | | <u>PAGE</u> |
|---------------|--|-------------|
| 1 | Typical MOSFET Noise Behavior | 5 |
| 2 | Shift in Low Frequency Noise Corner of a Buried Channel MOSFET Compared to a Surface Channel MOSFET | 14 |
| 3 | Typical Experimentally Measured Surface Channel and Buried Channel Noise Spectra | 17 |
| 4 | Cross-Sectional Drawing of Typical Buried Channel MOSFET and CCD Structures | 19 |
| 5 | Comparison of Surface Channel and Buried Channel MOSFET I-V Characteristics | 22 |
| 6 | Buried Channel Pinch-off Achieved With the Application of Substrate Bias | 24 |

LIST OF ILLUSTRATIONS

(continued)

| <u>FIGURE</u> | | <u>PAGE</u> |
|---------------|---|-------------|
| 7 | Effect of Backgate Bias Voltage on Buried Channel I-V Characteristics | 26 |
| 8 | Surface Channel and Buried Channel MOSFET Channel Potential (ϕ_{Max}) as a Function of Gate-to-Source Voltage (V_{GS}) | 27 |
| 9 | Source-Follower Method for Measuring ϕ_{Max} | 28 |
| 10 | ϕ_{Max} As a Function of Gate-to-Source Voltage and Gate Oxide Thickness | 29 |
| 11 | Surface Channel MOSFET Noise Characteristics as a Function of W/L Ratio | 33 |
| 12 | Buried Channel MOSFET Noise Characteristics as a Function of W/L Ratio | 34 |
| 13 | Buried Channel MOSFET Noise Characteristics as a Function of Gate Oxide Thickness | 36 |
| 14 | Buried Channel MOSFET White Noise Characteristic as a Function of Gate Oxide Thickness | 37 |
| 15 | Buried Channel Noise Characteristics as a Function of Ion Implant Drive-In Time | 38 |
| 16 | Buried Channel White Noise As a Function of Drive-In Time | 40 |
| 17 | Buried Channel MOSFET Noise Characteristics as a Function of Drain Current | 41 |
| 18 | Buried Channel MOSFET Noise Characteristics as a Function of Temperature | 43 |
| 19 | Surface Channel MOSFET Noise as a Function of Gate Area | 44 |
| 20 | Buried Channel MOSFET Noise Characteristics as a Function of Gate Area | 46 |
| 21 | Noise Characteristic of Interdigitated Buried Channel MOSFET Used in the First Stage of the Preamplifier | 47 |
| 22 | Interdigitated MOSFET Layout | 48 |
| 23 | Linear In-Line and Serpentine MOSFET Layouts | 50 |
| 24 | Buried Channel MOSFET Low Frequency Noise Characteristics as a Function of Gate Oxide Thickness | 51 |
| 25 | Low Frequency Noise of the Buried Channel MOSFET as a Function of Implant Drive-In Time | 52 |

LIST OF ILLUSTRATIONS

(continued)

| <u>FIGURE</u> | | <u>PAGE</u> |
|---------------|---|-------------|
| 26 | Buried Channel Poly-Si and Aluminum Gate MOSFET Noise Characteristics | 54 |
| 27 | Buried Channel Low Noise MOS Preamplifier | 58 |
| 28 | Preamplifier Bias Levels | 61 |
| 29 | Gain of Buried Channel Preamplifiers | 62 |
| 30 | Noise Measurement Set-Up | 64 |
| 31 | Buried Channel MOS Preamplifier Noise Characteristic | 65 |
| A-1 | Implanted Resistor Curves and MOSFET Curves for Figure A-4(b) Circuit | 72 |
| A-2 | Implanted Resistor | 72 |
| A-3 | Feedback Amplifier | 73 |
| A-4 | Buried Channel MOSFET Resistive Load Arrangements | 74 |
| A-5 | I-V Curves Corresponding to Figure A-4(a) Circuit | 74 |
| A-6 | MOSFET I-V Linearizing Technique for Implementing Integrated Resistors | 76 |
| A-7 | Curves for Circuit in Figure A-6 | 76 |
| A-8 | Superposition of Figures A-1 and A-5 to Yield A-8 Linear Characteristic of Figure A-7 | 77 |
| B-1 | Noise Measurement Test Station | 80 |
| B-2 | MOSFET Noise Test Box | 81 |
| B-3 | Photograph of Low Noise Test Fixture and Measuring Equipment | 82 |
| B-4 | Photomicrograph of the Low Noise Buried Channel MOSFET Preamplifier Test Bar. | 83 |

SECTION I INTRODUCTION

A. Background

Rapid advances have been made during the past several years in MOSFET and CCD technology. These advances have had a significant impact on many military signal processing functions found in such applications as forward-looking infrared (FLIR), radar, guidance and control, ECM, and sonar systems.¹⁻¹⁰ Particular attention has been focused on the development of the MOSFET and CCD technology for a CCD image buffer that could replace the electro-optical multiplexing hardware consisting of emitter module, emitter normalization board, adapter ring, collimator module, camera optics, and camera in a parallel-scanned FLIR system. This technology development effort has, in large part, been funded by the Air Force Avionics Laboratory under Contract No. F33615-73-C-1287.

In light of the successful demonstration of the CCD image buffer concept in a parallel-scanned FLIR breadboard system, the next logical step in the MOSFET and CCD technology development for this system application would be to evaluate the integration of all the interface amplifier circuitry directly on the image buffer array, thereby eliminating the need for the preamplifier and post-amplifier modules. For this system configuration the preamplifier noise must be less than the detector noise so the detector-noise-limited performance is maintained. Hence, in terms of this noise consideration, the integration of a low noise preamplifier onto the image buffer array presents severe constraints on MOSFET technology.

The typical surface channel MOSFET exhibits low frequency noise performance limitations for this application, and the low frequency noise problems associated with this device structure cannot be resolved merely with low noise circuit design techniques. Consequently, another device structure that will meet the low frequency noise requirement and be compatible with MOSFET and CCD fabrication techniques is required for the image buffer array.

In their work on noise mechanisms in buried channel CCD structures, Brodersen and Emmons¹¹ stated that a critical component for low noise CCD operation was the low noise MOSFET output buffer stage, which was processed with buried channel CCD technology. Their work experimentally demonstrated that the low frequency noise corner of a buried channel MOSFET was more than an order of magnitude lower than that of an identical surface channel MOSFET. In the buried channel MOSFET the conducting current is buried in the bulk silicon away from the silicon - silicon dioxide surface states and associated "1/f" noise. Therefore, the buried channel MOSFET structure has the potential of providing low frequency noise levels far superior to those of the surface channel device while maintaining process compatibility with MOSFET and CCD technology.

A need exists for further development of low noise buried channel MOSFET technology. In particular, the relationship of device noise performance to various geometric, process, and bias parameters needs to be clearly established. A detailed analysis of this structure as applied to low noise preamplifier design and development is also required, particularly in light of the large threshold voltage shifts encountered with the implanted device and the required substrate bias conditions for low current devices. Technological improvements in these areas could have a major impact on many low noise MOSFET and CCD technology applications such as the CCD image buffer. Therefore, this program focused attention on the low noise buried channel MOS preamplifier technology development.

B. Objective

The objective of this contract was to develop low noise buried channel MOSFET preamplifier technology that would allow the amplifier interface circuitry to be integrated on the CCD image buffer array. This effort was divided into two major thrusts.

First, the design and evaluation of buried channel MOSFET structures were conducted to obtain sufficient noise data on the white and the low frequency

noise levels for various geometric, process, and bias parameters. The typical CCD image buffer fabrication process was used with changes in only the ion implant drive-in time and gate oxide thickness. These buried channel devices were fully characterized in both the white and the low frequency noise regions as a function of the above mentioned parameters. The second thrust was to evaluate an integrated low noise buried channel MOSFET preamplifier. The overall noise characteristics of this preamplifier are dictated by the existing preamplifier module characteristics. These two major efforts are discussed in the following subsections.

Section II of this report is an overview of MOSFET noise theory, discussing the white noise and the low frequency noise regions. The mechanisms responsible for the noise phenomena in surface and buried channel devices are cited.

Section III presents experimental results of the MOSFET noise measurements for both surface and buried channel structures in terms of noise dependence on geometric, process, and bias parameters. These data are compared to theory, and deviations are cited. Particular attention is given to the large value of low frequency noise associated with the buried channel MOSFET that has an interdigitated source-drain structure.

In Section IV, the preamplifier circuit design is discussed. The experimental results of this integrated MOSFET preamplifier circuit are specified in terms of amplifier noise characteristics and performance parameters.

The last section contains a summary of the major conclusions drawn from the experimental noise data of Section III and the experimental observations concerning the preamplifier evaluation in Section IV as they apply to CCD image buffer technology.

Appendix A contains a discussion of a novel linear load resistor implementation which overcomes the linearity problems encountered with conventional MOSFET active load elements.

SECTION II

OVERVIEW OF MOSFET NOISE THEORY

The noise characteristics of the buried channel MOSFET in the first stage of the low noise preamplifier normally determine the noise equivalent voltage of the circuit. The spectral density of the noise equivalent voltage of MOSFET noise, e_n , can be separated into three distinct regions. In this effort only two are of interest, as indicated in Figure 1. As shown, the flat portion of the spectral density curve is called the white, thermal, or Johnson-Nyquist (J-N) noise region. The low frequency region is generally referred to as the low frequency noise, or the 1/f noise region. In the discussions that follow the white and low frequency terms are normally used to describe the regions. So that a clear comparison can be easily made between surface channel and buried channel MOSFET noise characteristics, a brief overview of MOSFET noise theory is given in this section.

In the MOSFET noise discussion that follows, a convenient way of expressing the key parameters that influence the noise spectrum, both white and low frequency regions, is through the use of the following generalized form:

$$e_n \propto f(F_1, F_2, F_3)$$

where F_1 = geometric parameter,

F_2 = process parameter, and

F_3 = bias parameter.

These generalized parameters are extremely useful in discussing the factors that predominantly influence MOSFET noise characteristics. As readily observed, the geometric parameters are controlled during the layout design of the MOSFET. The process parameters are governed during the fabrication of the device, while the bias parameters are set by the amplifier biasing configuration. The following discussion of MOSFET noise makes use of these three parameter for both surface and buried channel noise characteristics in the white and 1/f noise regions. The surface channel MOSFET noise theory for the white noise region is

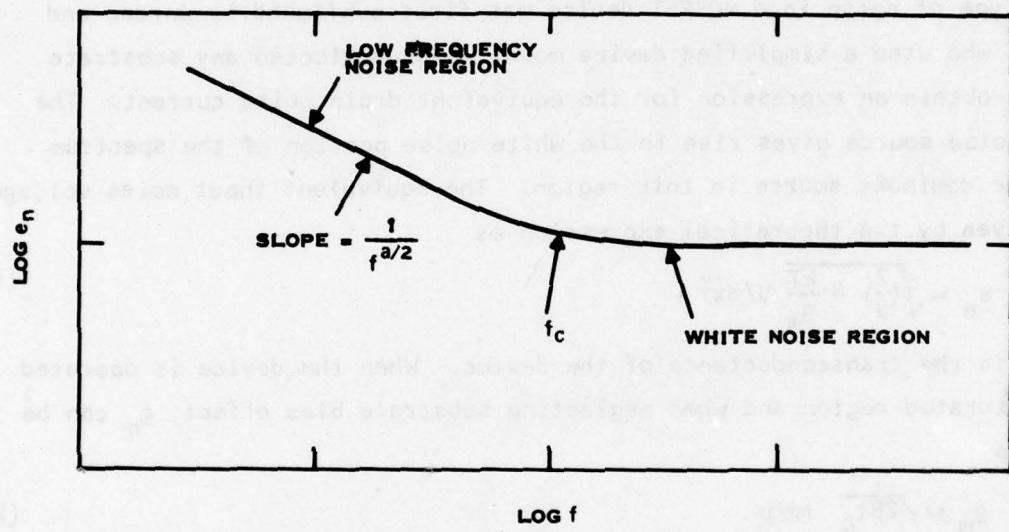


Figure 1. Typical MOSFET Noise Behavior

considered first, since the mechanisms responsible are closely related to both surface and buried channel structures.

A. White Noise

1. Surface Channel MOSFET

The white noise generated in the surface channel device is caused by random thermal motion of charge carriers in the conducting medium. An analysis of this type of noise in a MOSFET device was first published by Jordan and Jordan,¹² who used a simplified device model which neglected any substrate effect to obtain an expression for the equivalent drain noise current. The thermal noise source gives rise to the white noise portion of the spectrum and is the dominant source in this region. The equivalent input noise voltage, e_n , is given by the theoretical expression as

$$e_n = \sqrt{\left(\frac{2}{3}\right) 4 \frac{kT}{g_m}} \text{ V/Hz}^{\frac{1}{2}} \quad (1)$$

where g_m is the transconductance of the device. When the device is operated in the saturated region and when neglecting substrate bias effect, g_m can be written as

$$g_m \approx \sqrt{2\beta I_D} \text{ mhos} \quad (2)$$

where I_D is the dc drain-to-source current and β is given as

$$\beta \approx \frac{\mu \epsilon_{ox}}{t_{ox}} \left(\frac{W}{L}\right) \text{ mhos/V} \quad (3)$$

W and L are the width and length of the device, respectively. Combining Equations (2) and (3) with Equation (1), the equivalent input noise is expressed as being proportional to

$$e_n \propto \frac{(T)^{\frac{1}{2}}}{\left[\left(\frac{\mu}{t_{ox}}\right) \left(\frac{W}{L}\right) I_D\right]^{\frac{1}{4}}} \quad (4)$$

From Equation (4), the term in the denominator shows that the geometric dimensions of the device (W/L ratio) influence e_n by a minus fourth-root dependence, as does the drain current. That is, one or both of these parameters must be increased to decrease e_n . However, for the image buffer application, there is a practical limit on the amount the W/L ratio and I_D can be increased. As noted, the mobility, oxide thickness, and temperature also influence noise. Oxide thickness can be decreased for a low noise device, but again, practical considerations (development of pinholes) limit this decrease.

The measured thermal noise data can be much larger than that predicted from the above theory.¹²⁻¹⁵ For instance, substrate doping has an important effect on the thermal noise level, as verified by Sah.¹⁴ However, Halladay and Van der Ziel¹⁵ have shown that there are serious discrepancies between theory and experimental measurements even when the substrate effect is properly considered. It was postulated that a white noise source of nonthermal origin, which might arise from the interaction of carriers in the channel with ionized impurities, could account for the increased level of noise. Although the results of different authors are not in exact agreement, expression (4) clearly shows the dominant parameters that influence the white noise of a surface channel MOSFET and provide a reference for data interpretation. As noted in expression (4), each of the three generalized parameters, i.e., F_1 , F_2 , and F_3 , influences the white noise of a surface channel MOSFET. Hence, the generalized expression can be written as

$$e_n \propto F_1 (W, L) F_2 (\mu, t_{ox}) F_3 (I_D, T) \quad (5)$$

The functional relationship of surface channel white noise characteristics as a function of the generalized parameters is summarized in Table I.

2. Buried-Channel MOSFET

The surface channel white noise theories cited above indicate that the buried channel white noise characteristics should follow closely with the

TABLE 1
SURFACE CHANNEL MOSFET WHITE NOISE CHARACTERISTICS
AS A FUNCTION OF THE GENERALIZED PARAMETERS

| Parameter | Functional Relationship |
|--------------------------------|---|
| Geometric - W/L | $(W/L)^{-\frac{1}{4}}$ |
| Process - $\frac{\mu}{t_{ox}}$ | $(\mu)^{-\frac{1}{4}} (t_{ox})^{\frac{1}{4}}$ |
| Bias - $\frac{I_D}{T}$ | $(I_D)^{-\frac{1}{4}} (T)^{\frac{1}{2}}$ |

same functional relationship of the g_m of the device. When comparing the white noise behavior of surface channel and buried channel devices of equivalent geometry and bias current, Equation (1) predicts a higher level of noise for the buried channel device. This is primarily due to the lower g_m of the buried channel device. As seen from Equations (2) and (3), mobility and gate oxide thickness are the parameters that affect g_m for equivalent geometry devices and bias current. Comparing the higher bulk mobility of the buried channel device to the surface mobility of the surface channel device, a higher g_m is expected and therefore a lower white noise if t_{ox} and all other parameters are held constant. However, closer analysis reveals a difference in "effective" gate oxide thickness. In the surface channel device the conductive channel is at the silicon - silicon dioxide interface, with the gate being a distance from the channel determined primarily by t_{ox} . In contrast, the implanted channel in the buried channel MOSFET is separated from the controlling gate not only by the gate oxide thickness, but also by a portion of the thickness of the depletion layer between the silicon surface and the silicon bulk channel. The "effective" gate oxide thickness is therefore greater in a buried channel device, thus decreasing g_m . The increase in g_m due to bulk mobility is usually not sufficient to compensate for the greater distance of the controlling gate from the channel. This degradation in g_m in the buried channel MOSFET can be significant for deep ion implant devices. Under these conditions, device design with larger W/L and/or thinner gate oxide can be used to regain g_m . However, g_m can also be partially regained with shallow buried channel implant level. Hence, based upon Expression (4), Table I can be used to give the parameter relationships for buried channel white noise with ion implant depth added to the process parameter, F_2 .

B. Low Frequency Noise

The most dramatic noise improvement realized by using buried channel MOSFETs is manifested in the 1/f noise regions of the MOSFET noise spectrum. However, before the 1/f buried channel noise characteristics are discussed, a brief review

of the generally accepted 1/f surface channel noise theory is presented for comparison.

1. Surface Channel MOSFET

The low frequency noise in the surface channel MOSFET device is caused mainly by random fluctuations of carriers in the fast-interface surface states located at the oxide-semiconductor interface. Although a number of authors¹⁶⁻³⁰ have discussed the characteristics of surface-state noise in the MOSFET, no closed form solution has yet been achieved, mainly because of difficulties in obtaining a unique relation to the processing of the device. Possibly the most reasonable explanation is based on the modification of a noise model originally introduced by McWhorter¹⁷ for the explanation of flicker or 1/f noise in bulk semiconductors. This modification has been extensively evaluated by other investigators^{18,19} under the assumption that the noise is caused by a random trapping of free carriers in the fast-interface surface states. To provide the required 1/f frequency response, the trapping is supposed to occur via a tunneling mechanism. This, then, gives rise to the low frequency fluctuation in the channel current with a $(1 + \omega^2 \tau^2)^{-1}$ dependence.

Following the modified McWhorter approach, Klassen²¹ concluded from his theoretical and experimental results that the equivalent input noise voltage in the low frequency region is proportional to the square root of the gate voltage and fast-interface surface state density, N_{ss} , and inversely proportional to the square root of the gate area, A_g . Other investigators such as Fu and Sah²⁴ have taken different approaches for the explanation of this noise by modifying and expanding on previous theories. Others^{25,26} have established different theoretical approaches. Regardless of their findings, experimental observations have provided supporting evidence that there are several important features that are common to the above-mentioned theories. Summarizing their findings, the key factors that influence the 1/f noise spectrum for surface channel MOSFETs can be stated in a manner as discussed by Ronen.²⁷ The generalized expression for low frequency noise can take the following form:

$$e_n \propto F_1 (W, L) F_2 (t_{ox}, N_{ss}) F_3 (V_{GS})$$

The geometry parameter, F_1 , influences e_n through the relation given by

$$e_n \propto \frac{1}{\sqrt{WL}} = \frac{1}{\sqrt{A_g}}$$

Hence, e_n will be decreased by an increase in gate area, A_g . However, the maximum area will be limited by the gain-bandwidth considerations and the limitations in silicon real estate.

The principal factors in the process parameter, F_2 , are gate oxide thickness and fast surface-state density, N_{ss} . The dependence of e_n on gate oxide thickness can range from square root to linear. For thicker oxides, the observed dependence tends to be more linear, whereas for thinner oxides, e_n has been observed to decrease with oxide thickness more than expected. However, the minimum oxide thickness will be limited by pinhole density and dielectric breakdown. That is, the oxide cannot be so thin as to result in device reliability problems, and high quality thin gate oxides are required. The fast surface-state density, N_{ss} , is probably the most important parameter in controlling the lowest possible value of $1/f$ noise, since the noise spectral density is predicted to be proportional to N_{ss} . Furthermore, the type of gate material has been observed to have an effect on the low frequency noise characteristics.

The bias factor, F_3 , does not influence the low frequency noise as much as the other two factors. Low frequency noise is almost independent of drain voltage and drain current; however, a dependence on the effective gate-to-source voltage, V_{GS} , has previously been shown to have somewhat of a square root to linear effect. Devices with low density and uniform distribution of fast interface state traps have little dependence on low frequency noise with temperature.^{20,26} Note however that thermal noise decreases with an increase in drain current. Table 2 summarizes the parametric relationships that appear to have the major influence on low frequency noise in surface channel MOSFETs.

TABLE 2
SURFACE CHANNEL LOW FREQUENCY NOISE CHARACTERISTICS
AS A FUNCTION OF GENERALIZED PARAMETERS

| Parameters | Functional Relationship |
|------------------------|---|
| Geometric - A_g (WL) | A_g^{-2} |
| Process - t_{ox} | $t_{ox} \rightarrow t_{ox}^2$ |
| N_{ss} | N_{ss} |
| Bias - V_{GS} | $V_{GS}^{\frac{1}{2}} \rightarrow V_{GS}$ |

2. Buried Channel MOSFET

As stated earlier, a dramatic reduction of noise in the low frequency spectrum can be realized by using the buried channel MOSFET devices. This device structure essentially moves the current flow away from the "noisy" surface, thus reducing the effect of surface interaction, and consequently reducing surface state 1/f noise components. Figure 2 illustrates the improvement in low frequency noise characteristics resulting from an implanted channel.¹¹ This figure shows that the shift in the noise corner is significant and can be related to a change in the mechanism responsible for low frequency noise phenomena in MOSFETs. As mentioned above, the surface channel mechanism is due to surface state trapping. In the buried channel MOSFET, however, the low frequency noise mechanism can be related to bulk phenomena, since the conducting channel has been moved away from the surface to the bulk region. More precisely, the low frequency noise mechanism in the buried channel MOSFET can be associated with generation-recombination (g-r) centers within the bulk. Although considerable effort has been devoted to the theory of low frequency noise mechanisms in surface channel MOSFETs, detailed theoretical considerations have not been completely developed for low frequency buried channel devices. A detailed discussion of the noise mechanism in buried channel low frequency noise is postponed until the experimental evaluation is given. However, previous work on bulk types of structures is used as the basis for the brief discussion of generation-recombination noise characteristics given below.

The g-r centers in the depletion region beneath the gate give rise to random emission and generation of electrons and holes. This causes fluctuation in the channel charge, thereby leading to a noise component in the drain current.³¹ The time constants associated with the g-r centers are extremely low^{32,33} and are much smaller than the surface-state 1/f noise. Since the significant noise source in the low frequency noise region is the g-r noise component, a much lower noise spectrum is realized. This component is primarily due to the residual damage induced the bulk substrate by the implantation process; consequently,

consequently with addition to surface channel a surface barrier diode effect. Results of this research indicate that noise in buried channel devices is not appreciable with respect to noise in surface channel devices. This is due to the fact that the noise in the surface channel is due to surface states, which are present in the surface channel, but are absent in the buried channel. The noise in the buried channel is due to the presence of g-r centers, which are present in the buried channel, but are absent in the surface channel. The noise in the surface channel is due to the presence of surface states, which are present in the surface channel, but are absent in the buried channel.

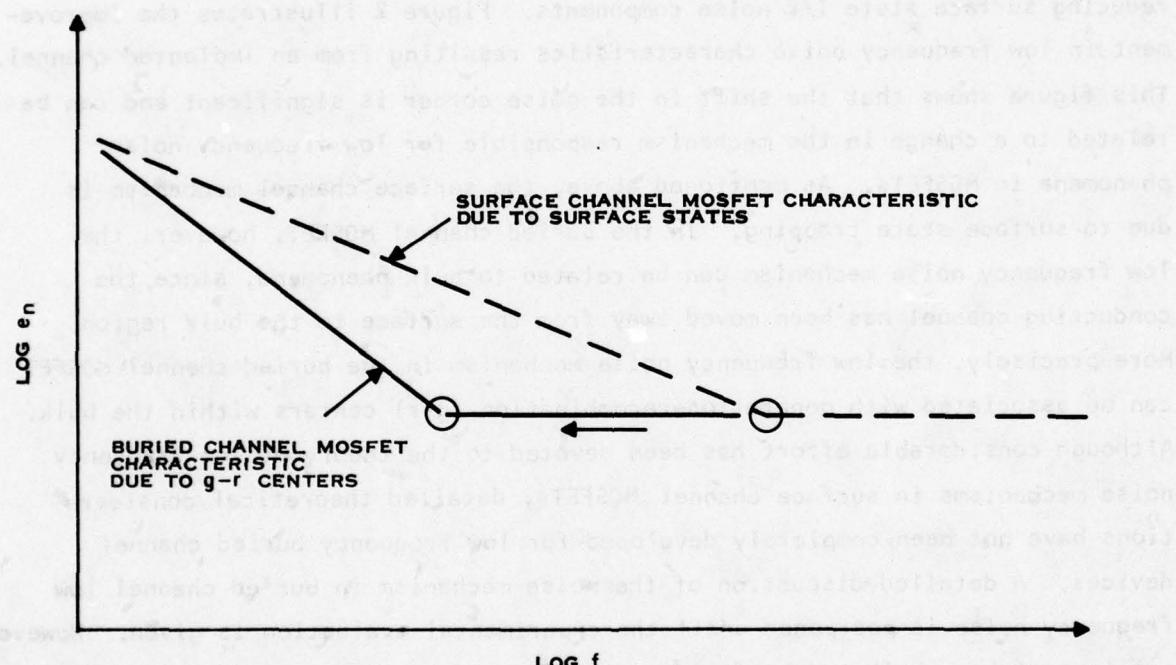


Figure 2. Shift in Low Frequency Noise Corner of a Buried Channel MOSFET Compared to a Surface Channel MOSFET

the ion implant depth should have a major influence on this low frequency noise spectrum. Conversely, the N_{ss} found in the generalized expression for the surface channel device should not be present, since the current flow is away from the surface-state noise centers. It is postulated that the gate oxide thickness will also influence the low frequency noise characteristics.

The low frequency noise voltage below the corner frequency increases as the frequency decreases by a rate that is proportional to $f^{\alpha/2}$. The g-r noise source gives rise to a value of approximately $\alpha = 2$. Hence, the slope is nearly twice as steep as the "true" 1/f spectrum as depicted in Figure 2.

In summary, the theoretical parameters that affect the white and low frequency noise behavior of surface and buried channel MOSFETs were used as a guideline, along with somewhat limited experimental buried channel MOSFET data, to design the MOSFET test structures and preamplifier circuit. The experimental MOSFET noise evaluation is discussed in the next section.

SECTION III
BURIED CHANNEL MOSFET EXPERIMENTAL
NOISE CHARACTERISTICS

Typical low frequency noise characteristics of a buried channel MOSFET are very much better than those of an identical surface channel MOSFET, as shown in Figure 3. As illustrated, implanting the channel of the MOSFET structure causes the corner frequency to decrease dramatically, to an even lower value than the surface channel device with an order of magnitude larger gate area. The corner frequency for the $A_g = 0.28 \text{ mm (11 mils)}$ decreases from approximately 100 kHz for the surface channel device to less than 2 kHz for the buried channel structure. This decrease in the corner frequency is nearly two orders of magnitude. Due to this large decrease in corner frequency, buried channel MOSFET noise characteristics lend themselves to many low frequency circuit requirements. Hence, one of the objectives of this contract was to evaluate the noise characteristics of this type of device and to compare buried channel and surface channel MOSFET noise characteristics.

This section contains a discussion of the experimental evaluation of the noise spectrum of surface channel and buried channel MOSFETs. Additional MOSFET noise data are also included, when appropriate, from evaluation of other MOSFET test structures, primarily surface channel or small geometry buried channel devices.

A brief description of the buried channel MOSFET fabrication technique is given in Section III.A, and Section III.B discusses the unique output current-voltage (I-V) characteristic of typical buried channel MOSFETs. Experimental data follow in the remaining subsections.

Since one of the objectives of this program was to experimentally characterize white and low frequency buried channel MOSFET noise spectra, surface channel devices are also evaluated for comparison. Both surface

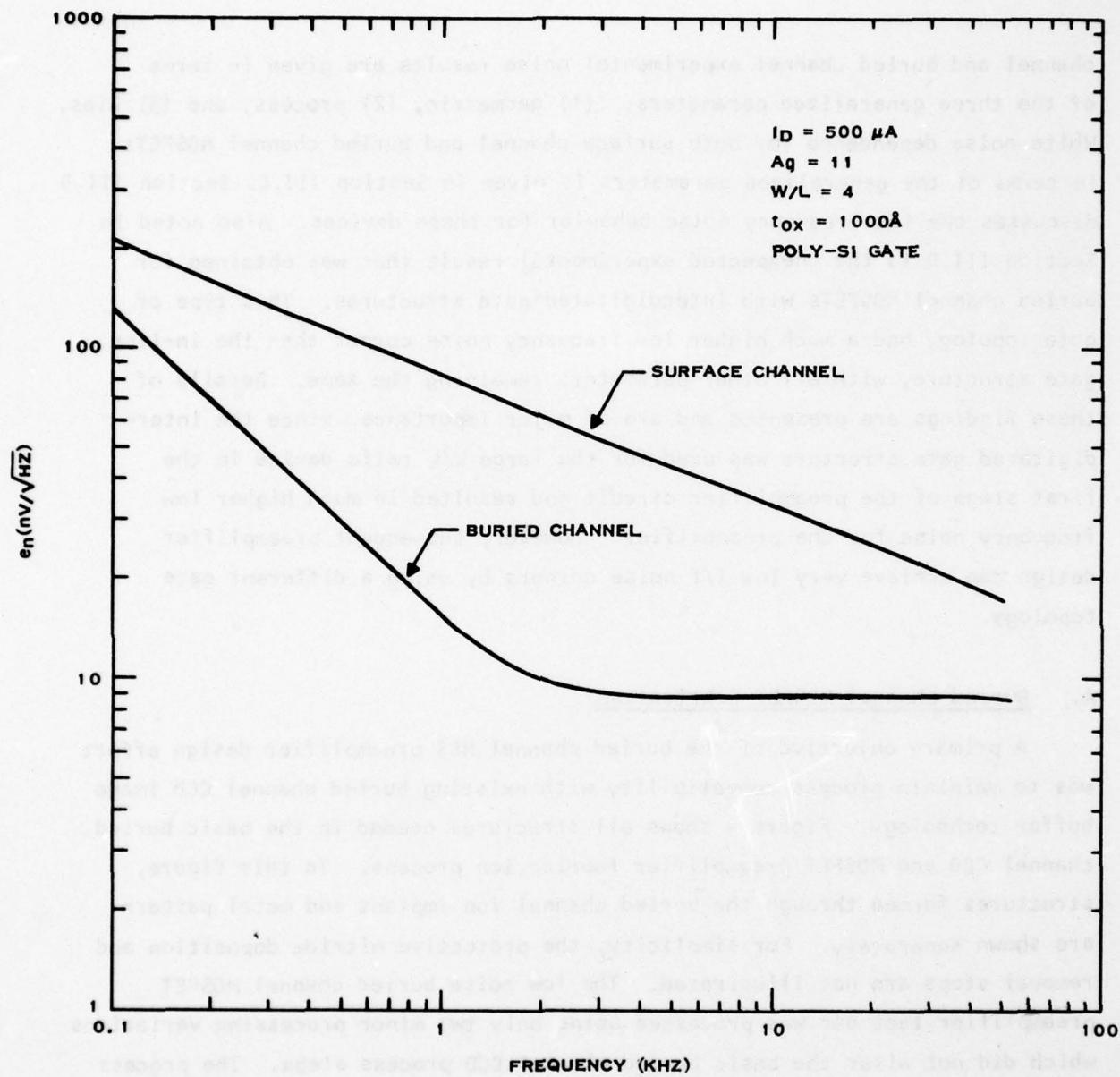


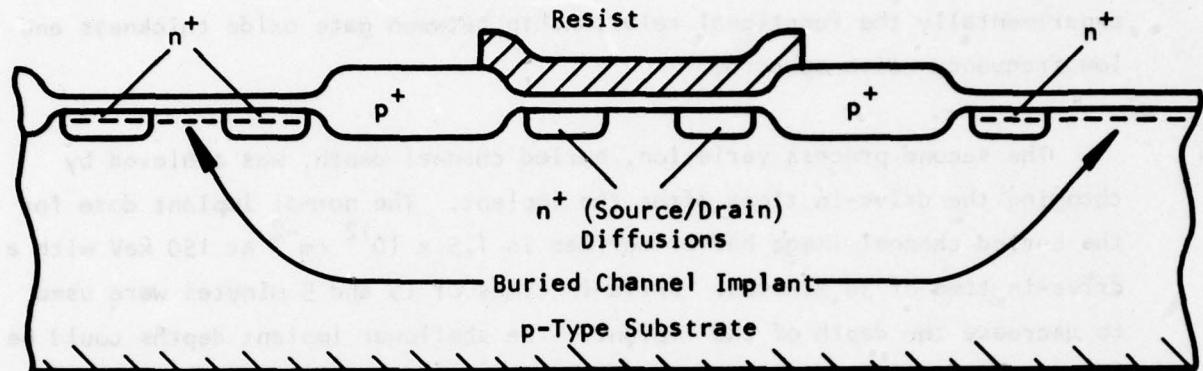
Figure 3. Typical Experimentally Measured Surface Channel and Buried Channel Noise Spectra

channel and buried channel experimental noise results are given in terms of the three generalized parameters: (1) geometric, (2) process, and (3) bias. White noise dependence for both surface channel and buried channel MOSFETs in terms of the generalized parameters is given in Section III.C. Section III.D discusses the low frequency noise behavior for these devices. Also noted in Section III.D is the unexpected experimental result that was obtained for buried channel MOSFETs with interdigitated gate structures. This type of gate topology had a much higher low frequency noise corner than the in-line gate structure, with all other parameters remaining the same. Details of these findings are presented and are of major importance, since the interdigitated gate structure was used for the large W/L ratio device in the first stage of the preamplifier circuit and resulted in much higher low frequency noise for the preamplifier. However, subsequent preamplifier design can achieve very low 1/f noise corners by using a different gate topology.

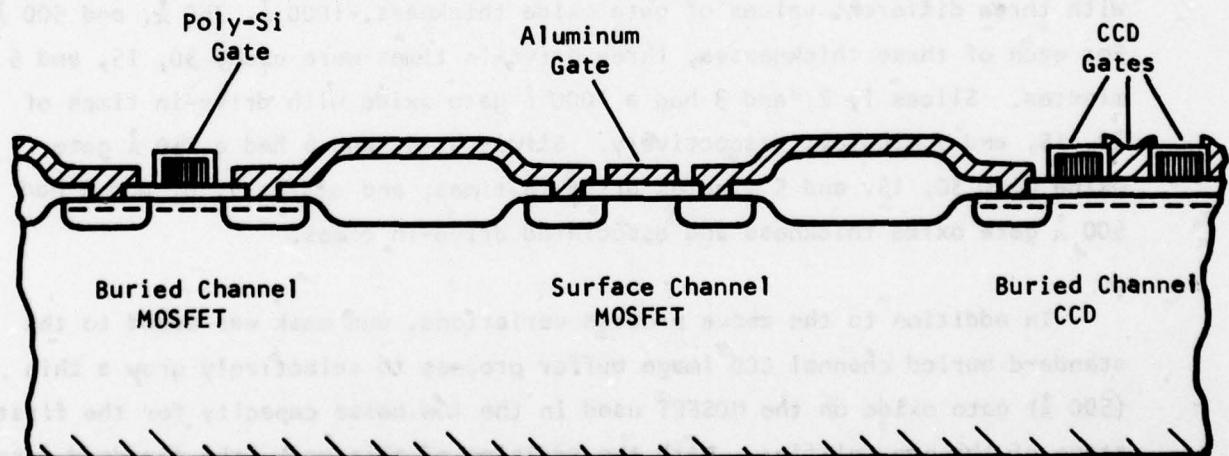
A. Buried Channel MOSFET Fabrication

A primary objective of the buried channel MOS preamplifier design effort was to maintain process compatibility with existing buried channel CCD image buffer technology. Figure 4 shows all structures needed in the basic buried channel CCD and MOSFET preamplifier fabrication process. In this figure, structures formed through the buried channel ion implant and metal pattern are shown separately. For simplicity, the protective nitride deposition and removal steps are not illustrated. The low noise buried channel MOSFET preamplifier test bar was processed using only two minor processing variations which did not alter the basic buried channel CCD process steps. The process variations, gate oxide thickness and ion implant drive-in time, were used to enhance the white and low frequency noise performance in buried channel MOSFETs. The particular process alterations chosen were based on noise theory as discussed in Section II.

structure of buried channel MOSFET. A need to reexamine the design with
minimum need for pulsed voltages to TEGO and difficulties of epitaxial and
ionized and to base of silicon to CCD. Present and research helped to
improve the design and reduce the cost of fabrication.



(a) Process Through Buried Channel Implant



(b) Process Through Metal Pattern

Figure 4. Cross-Sectional Drawing of Typical Buried Channel MOSFET and CCD Structures

Gate oxide thicknesses of 1000 Å, 750 Å, and 500 Å were used to evaluate the ability to reestablish the MOSFET g_m after its value had been lowered with the buried channel ion implant. The 1000 Å gate oxide is used as the typical thickness for CCD image buffer devices. It was important to determine experimentally the functional relationship between gate oxide thickness and low frequency noise spectrum.

The second process variation, buried channel depth, was achieved by changing the drive-in times after the implant. The normal implant dose for the buried channel image buffer devices is $1.5 \times 10^{12} \text{ cm}^{-2}$ at 150 keV with a drive-in time of 30 minutes. Drive-in times of 15 and 5 minutes were used to decrease the depth of the implant. The shallower implant depths could be a means of increasing the buried channel MOSFET g_m , thereby decreasing the white noise level. Also of interest was the anticipated effect of the buried channel ion implant depth in the low frequency noise level.

As stated above, the buried channel MOS preamplifier lot was processed with three different values of gate oxide thickness, 1000 Å, 750 Å, and 500 Å. For each of these thicknesses, three drive-in times were used, 30, 15, and 5 minutes. Slices 1, 2, and 3 had a 1000 Å gate oxide with drive-in times of 30, 15, and 5 minutes, respectively. Slices 4, 5, and 6 had a 750 Å gate oxide with 30, 15, and 5 minutes drive-in times; and slices 7, 8, and 9 had 500 Å gate oxide thickness and associated drive-in times.

In addition to the above process variations, one mask was added to the standard buried channel CCD image buffer process to selectively grow a thin (500 Å) gate oxide on the MOSFET used in the low noise capacity for the first stage of the preamplifier. With the addition of this mask, the standard gate oxide thickness could be maintained in large CCD structures by having the thin gate oxide thickness only for the first stage of the preamplifier circuits. Therefore, slice 10 in the lot was processed using the thin gate oxide mask to grow the 500 Å with gate oxide only on the preamplifier input MOSFET and several test MOSFETs while the standard gate oxide was used over the rest of the slice.

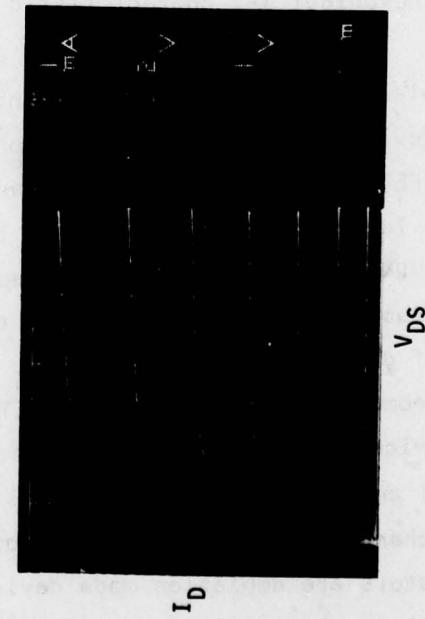
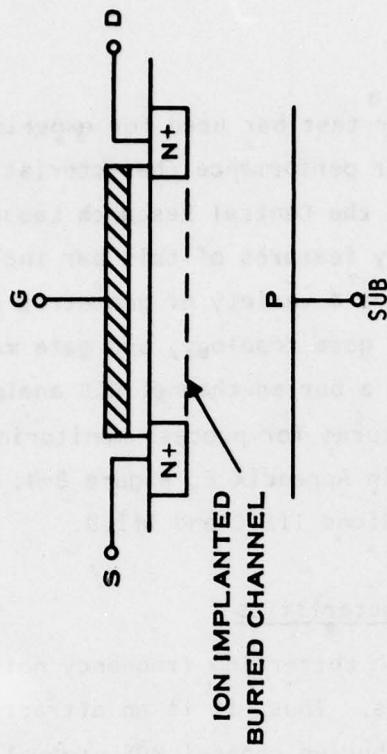
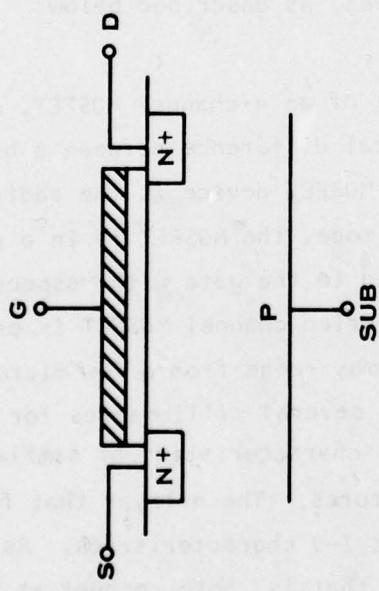
The buried channel MOSFET preamplifier test bar used for experimental evaluation of MOSFET noise and preamplifier performance characteristics was processed in the CCD pilot line located in the Central Research Laboratories at Texas Instruments Incorporated. Primary features of this bar include a number of test MOSFET structures that have a variety of geometric configurations in terms of W/L ratio, gate area, gate topology, and gate material; a buried channel MOS preamplifier circuit; a buried channel CCD analog memory test structure; and a number of test structures for process monitoring. The photomicrograph of this test bar is shown in Appendix B, Figure B-4. The noise evaluation of the test bar is given in Sections III.C and III.D.

B. Buried Channel MOSFET Output I-V Characteristics

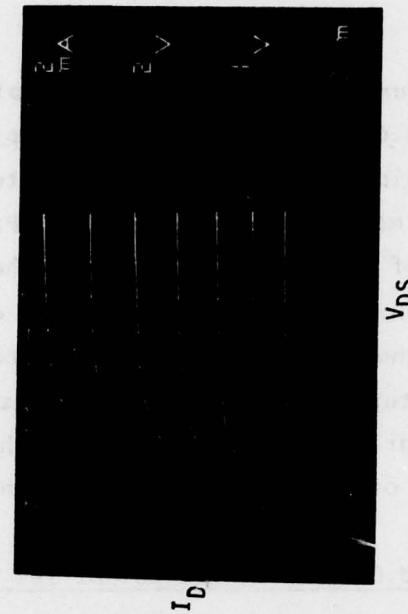
The buried channel MOSFET exhibits much better low frequency noise characteristics than surface channel devices. Thus, it is an attractive choice for use in implementing a low noise buried channel MOS preamplifier. However, the physical structure of this buried channel MOSFET is different from that of surface channel devices, and this difference has an important effect on the output I-V characteristic curves, as described below.

By implanting an n layer in the channel of an n-channel MOSFET, a depletion mode device is formed. The only physical difference between a buried channel MOSFET device and a surface channel MOSFET device is the addition of this n-type layer under the oxide. In this mode, the MOSFET is in a conducting or "ON" state with zero volts applied to the gate with respect to the source and substrate. The degree that the buried channel MOSFET is on, or the level of drain current, I_D , for $V_{GS} = 0$ may range from a few microamperes for small geometry buried channel MOSFETs to several milliamperes for large geometry devices. Figure 5 compares the I-V characteristics of similar surface channel and buried channel MOSFET structures. The n-layer that forms the buried channel modifies the MOSFET output I-V characteristics. As shown, both transistors are depletion mode devices; that is, both conduct at zero gate-to-source voltage, V_{GS} , with zero substrate bias voltage. However, the surface

NMOS STRUCTURES



SURFACE CHANNEL



BURIED CHANNEL

Figure 5. Comparison of Surface Channel and Buried Channel MOSFET I-V Characteristics

channel device indicates $I_D \approx 0$ for $V_{GS} = 0$, which effectively turns the device off. In contrast, the buried channel device for $V_{GS} = 0$ has a drain current of several hundred microamperes.

Another difference exists in the I-V characteristics of the buried channel MOSFET. This unusual characteristic of the buried channel depletion mode transistors is due to the n-layer at the silicon surface which connects the n-source and drain diffusions. These devices behave as diffused resistors for small drain-to-source voltages and zero gate bias. Since the n-layer extends an appreciable distance into the p-type substrate, conduction in these devices also extends into the bulk instead of occurring entirely along the surface, as in a surface channel MOSFET. This results in the unique characteristics of these transistors. As the gate voltage is increased in a negative direction, the depletion layer formed at the surface extends farther and farther into the n-layer, reducing the source-to-drain conductance. However, if the n-layer is sufficiently thick, the silicon surface under the gate will become inverted before the depletion layer extends through the implanted n-layer. Once the surface becomes inverted, the depletion layer is clamped at the value attained at inversion. At this point, there is still sufficient charge in the undepleted portion of the channel to sustain drain current. Under these conditions the gate-to-source voltage does not influence the drain current, and the device cannot be turned off with only V_{GS} .

To turn these buried channel devices off, the n-region underneath the gate electrode must be depleted. The voltage level of the source and drain diodes must be raised relative to the substrate. The p-n junction between the ion implanted n-layer and the p-type substrate is reverse-biased, and the junction depletion region extends upward from this junction toward the surface depletion region, as shown in Figure 6. If the junction depletion region is sufficiently large so that this region merges with the surface depletion region, the n-layer will be depleted and the device will be cut off.

which will result in a voltage of about -20 V and 0 m^2 of emission current. I assume that with $0 = -20$ V and $0 = 20$ V, the electrons formed behind the anode in the emission current will be emitted from the anode to the cathode.

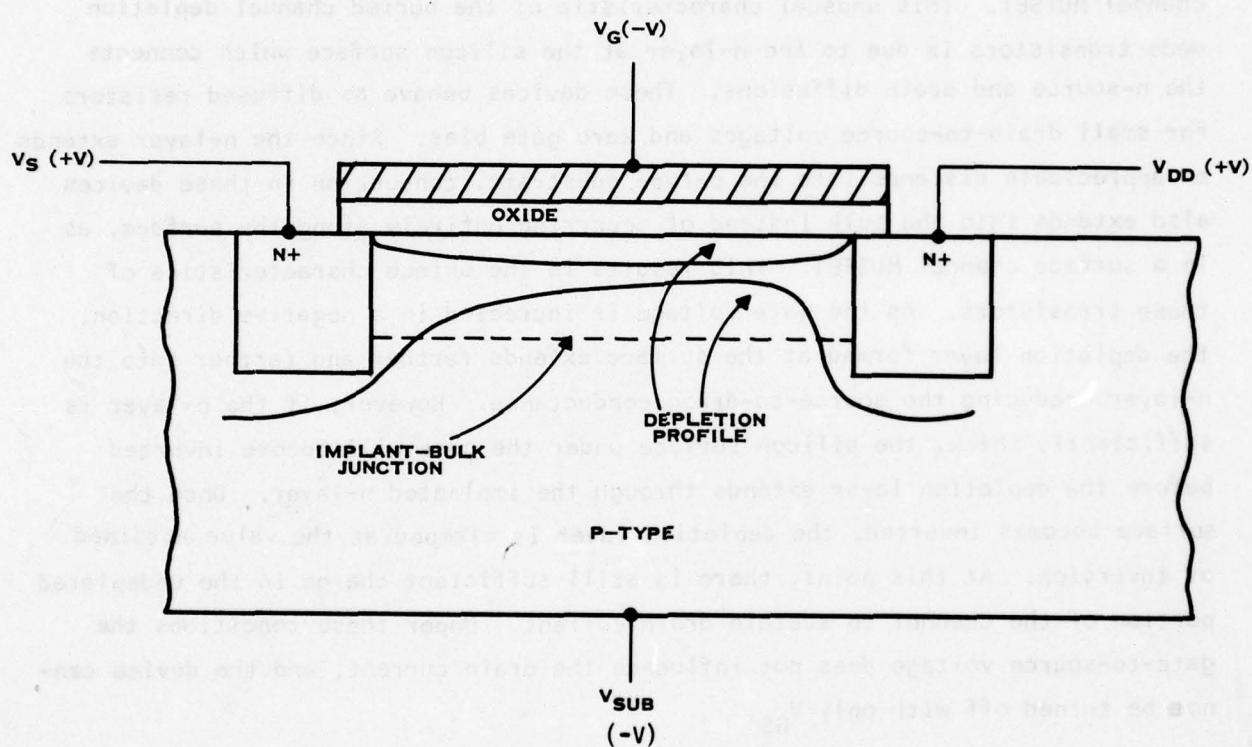


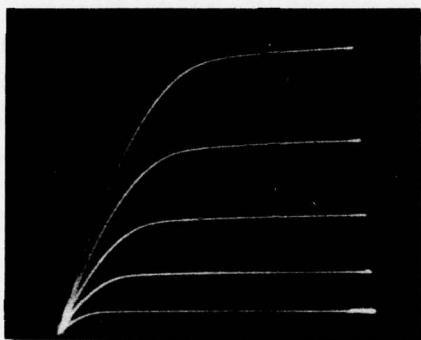
Figure 6. Buried Channel Pinch-off Achieved With the Application of Substrate Bias

By using a negative substrate bias voltage, the buried channel MOSFET I-V characteristics can be modified much as surface channel MOSFET I-V characteristics can be changed by using back gate bias.³⁴ Therefore, applying sufficient negative voltage to the substrate, V_{SUB} , to just pinch off the channel at $V_{GS} = 0$ makes low bias currents attainable and returns channel control to the gate voltage at the lower current levels. Figure 7 shows the effect of a device with substrate voltage, V_{SUB} , equal to 0, -3, and -6 V. Hence, a negative substrate voltage is required to operate the large W/L geometry buried channel MOSFET at low currents. However, a high g_m can be maintained when a near pinch-off bias point is achieved. The implication of this behavior is that for low values of drain current and sufficiently high values of g_m , the drain current can be controlled by the gate through use of a negative substrate voltage.

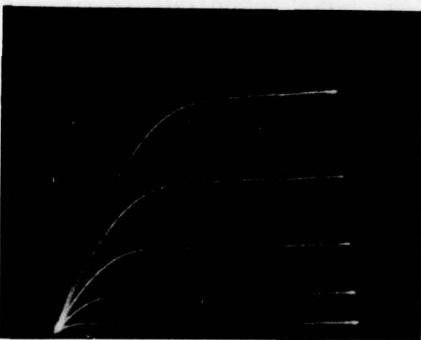
Another way of considering this phenomenon is illustrated in Figure 8. The measurement of the peak voltage in the channel, ϕ_{MAX} , can be used as an indication of the ion implant concentration. The ϕ_{MAX} , which is proportional to I_D , is plotted in this figure for equivalent geometry surface channel and buried channel devices. The source-follower method for measuring ϕ_{MAX} , developed by Tasch, et al.,³⁵ allows for an easy technique to measure ϕ_{MAX} , as illustrated in Figure 9. In the case of the surface channel device, ϕ_{MAX} is nearly zero for a value of gate-to-source voltage equal to zero. In comparison, the buried channel devices exhibit larger values of ϕ_{MAX} for $V_{GS} = 0$, which also implies a more negative threshold voltage, V_T , or deep ion implant. Even more noteworthy, the buried channel device ϕ_{MAX} curves saturate as V_{GS} is brought more negative. When this curve saturates, the gate-to-source voltage no longer controls the channel conductance; that is, g_m effectively goes to zero. For different values of ion implant concentration and depth, the saturation point of the ϕ_{MAX} varies. The ϕ_{MAX} curves as a function of gate voltage for slices 1 through 9 are shown in Figure 10. These curves were produced by using the same buried channel MOSFET structure. As illustrated in Figure 10(a)



(A) $V_{SUB} = 0$ VOLTS



(B) $V_{SUB} = -3$ VOLTS



(C) $V_{SUB} = -6$ VOLTS

Figure 7. Effect of Backgate Bias Voltage on Buried Channel I-V Characteristics

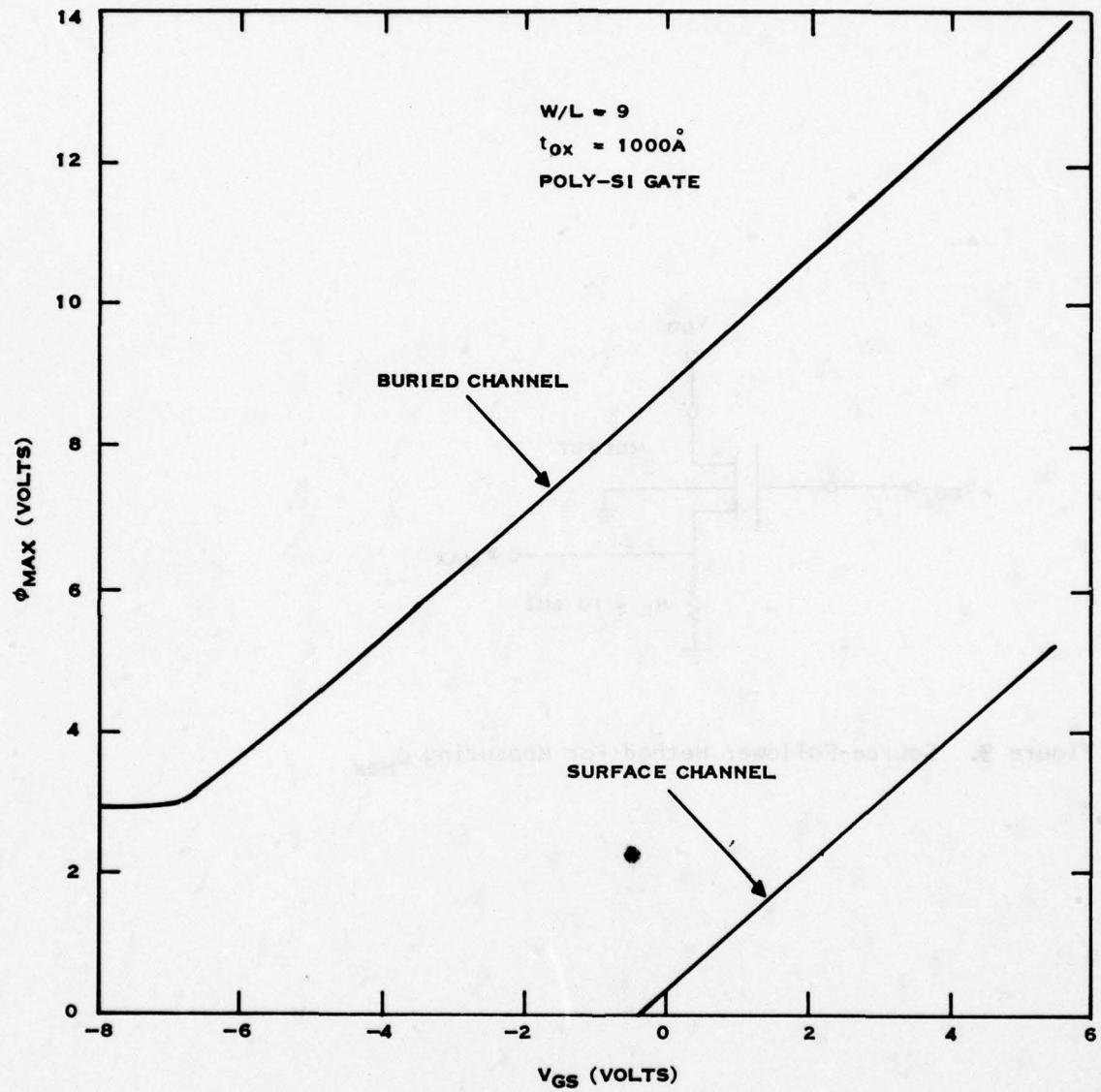


Figure 8. Surface Channel and Buried Channel MOSFET Channel Potential (ϕ_{MAX}) as a Function of Gate-to-Source Voltage (V_{GS})

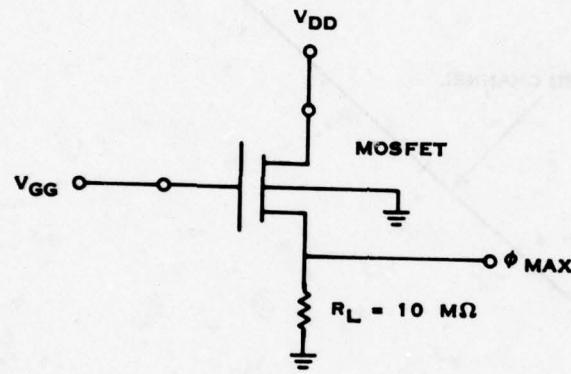


Figure 9. Source-Follower Method For Measuring ϕ_{MAX}

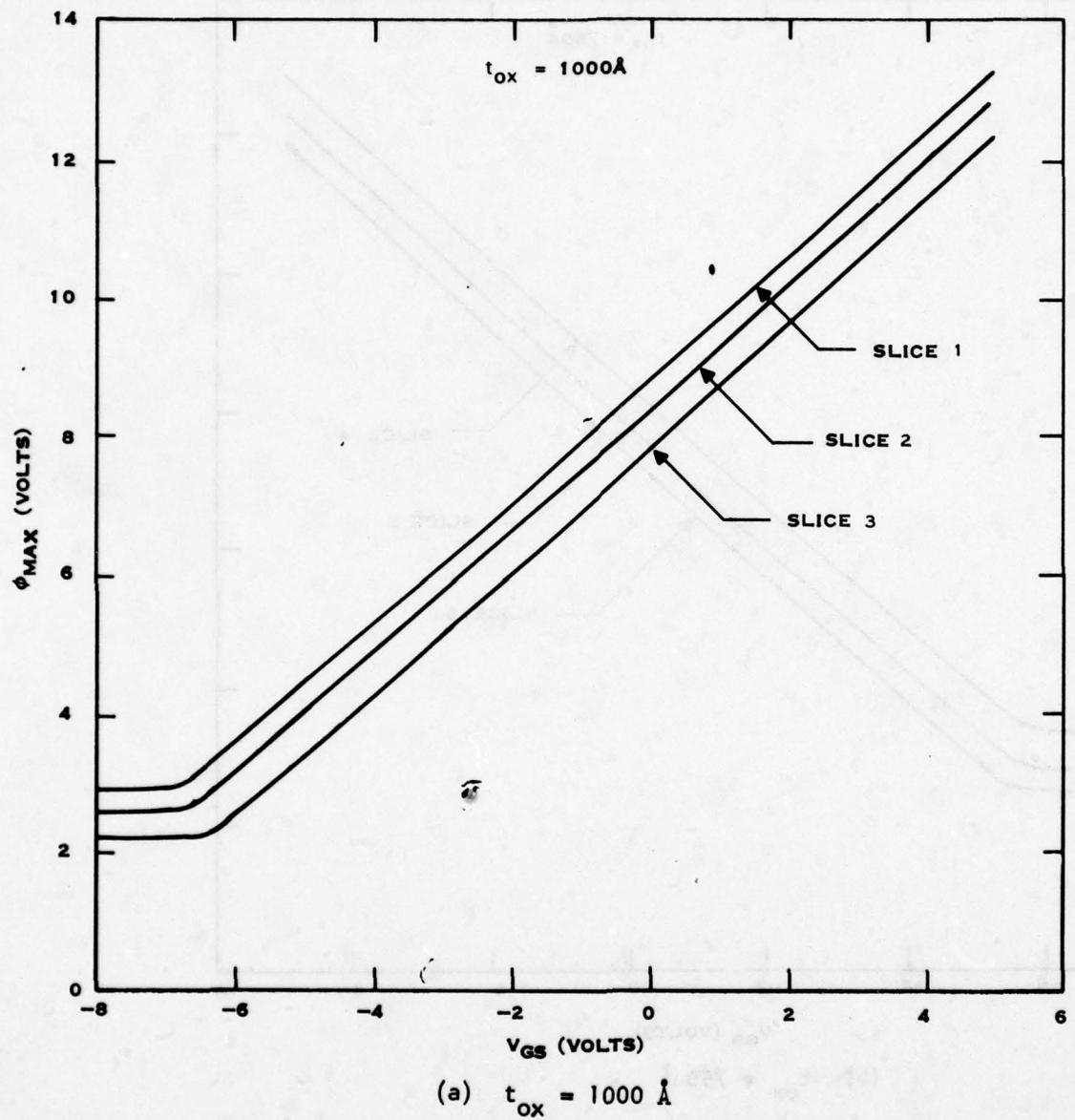


Figure 10. ϕ_{MAX} As a Function of Gate-to-Source Voltage and Gate Oxide Thickness

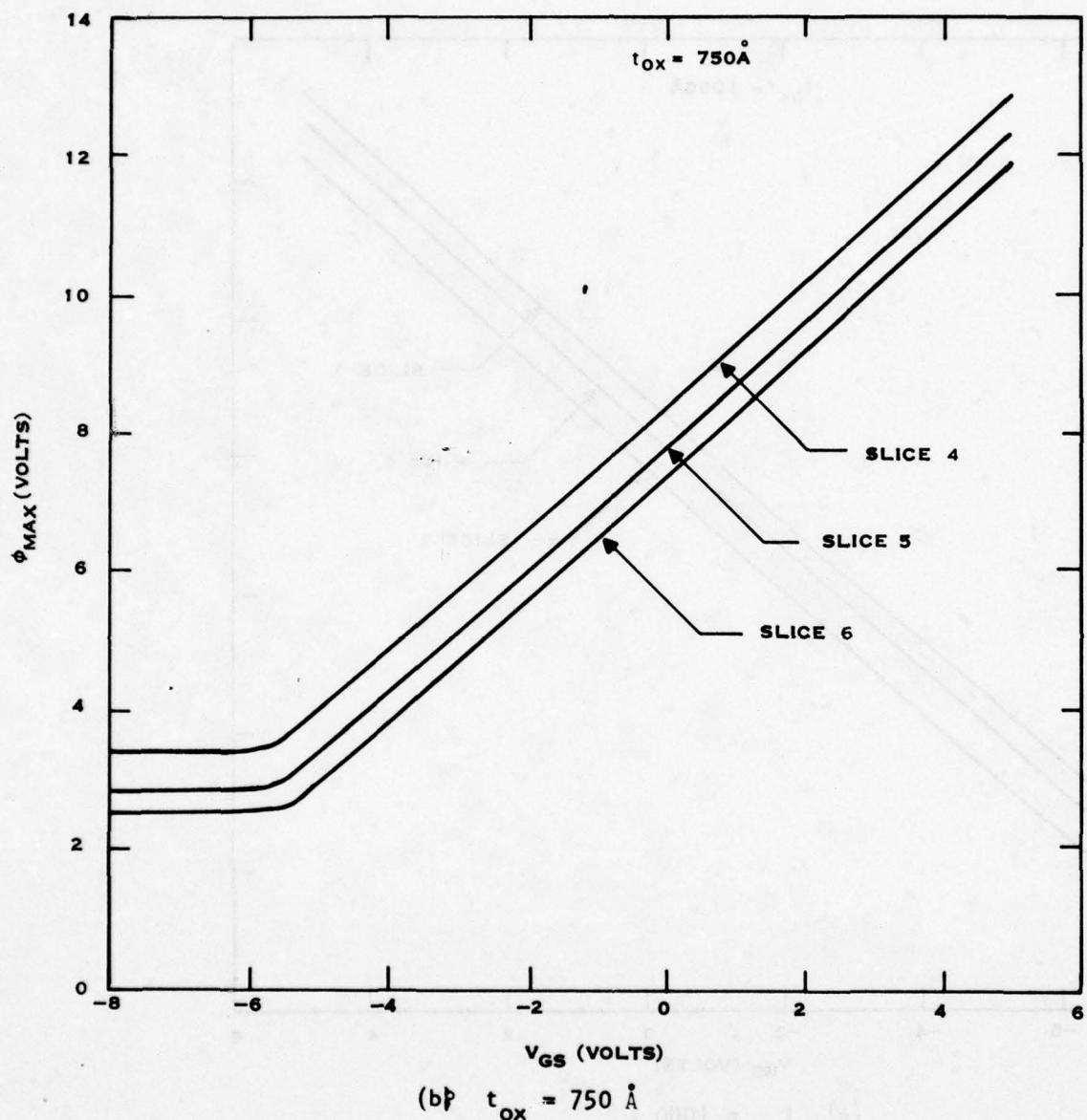


Figure 10. (continued)

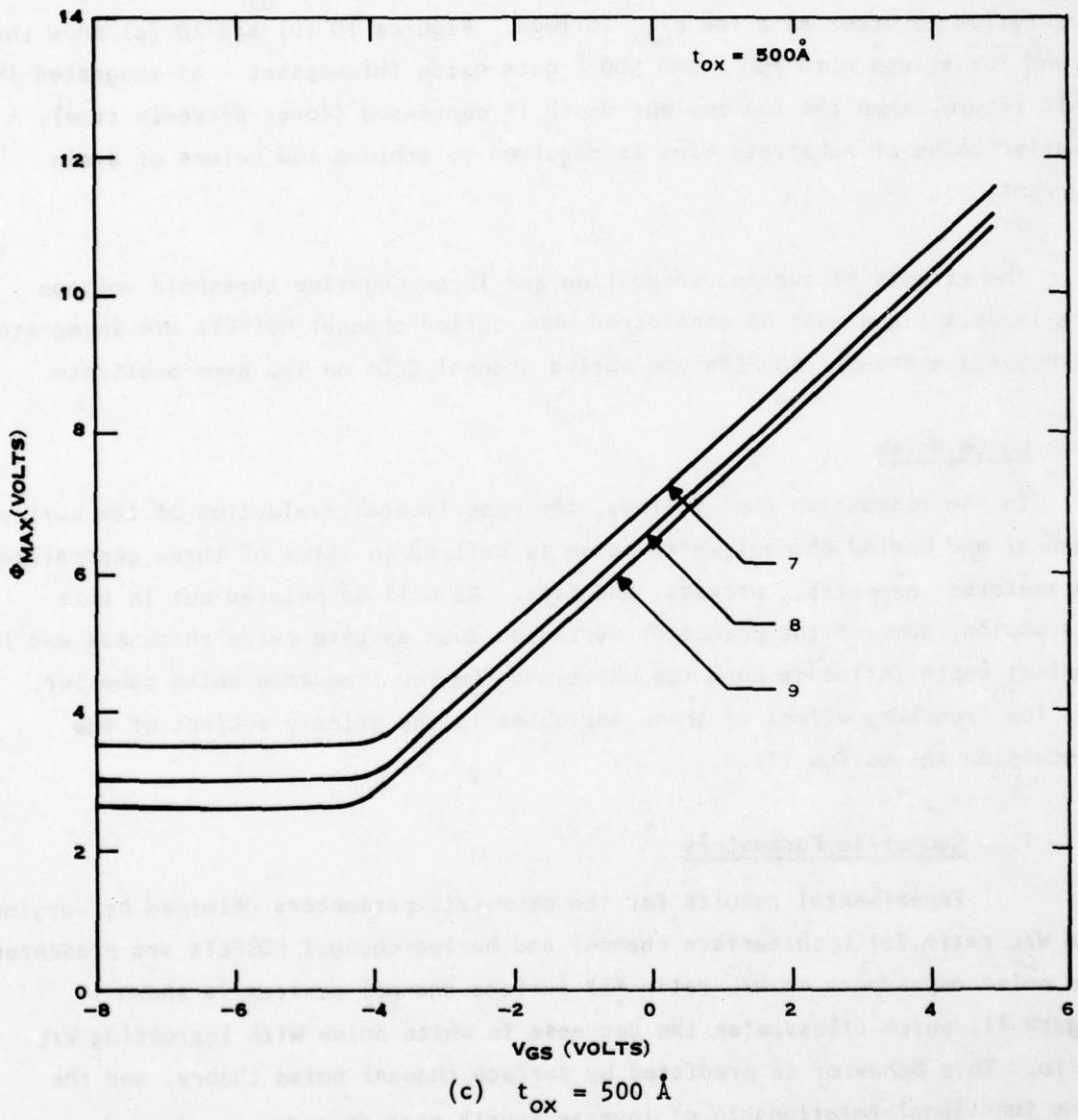


Figure 10. (continued)

with a gate oxide thickness of 1000 Å, as the drive-in time decreases, the ϕ_{MAX} curves shift downward, making ϕ_{MAX} less for a given V_{GS} and causing the saturation to occur at a low ϕ_{MAX} voltage. Figures 10 (b) and 10 (c) show the same trend for slices with 750 Å and 500 Å gate oxide thicknesses. As suggested in this figure, when the ion implant depth is decreased (lower drive-in time), a smaller value of substrate bias is required to achieve low values of drain current.

The effects of current saturation and large negative threshold voltage are important and must be considered when buried channel MOSFETs are integrated with surface channel MOSFETs and buried channel CCDs on the same substrate.

C. White Noise

In the discussion that follows, the experimental evaluation of the surface channel and buried channel white noise is defined in terms of three generalized parameters: geometric, process, and bias. As will be pointed out in this discussion, some of the parameter variables such as gate oxide thickness and ion implant depth influence both the white and the low frequency noise behavior. The low frequency effect of these variables is the primary subject of the discussion in Section III.D.

1. Geometric Parameters

Experimental results for the geometric parameters obtained by varying the W/L ratio for both surface channel and buried channel MOSFETs are presented. The noise dependence on W/L ratio for surface channel devices is shown in Figure 11, which illustrates the decrease in white noise with increasing W/L ratio. This behavior is predicted by surface channel noise theory, and the same functional relationship of inverse fourth-root dependence exists for buried channel devices, as illustrated in Figure 12. As shown, for a W/L ratio of 300 the white noise level is 3.5 nV/ $\sqrt{\text{Hz}}$, while for a W/L ratio of

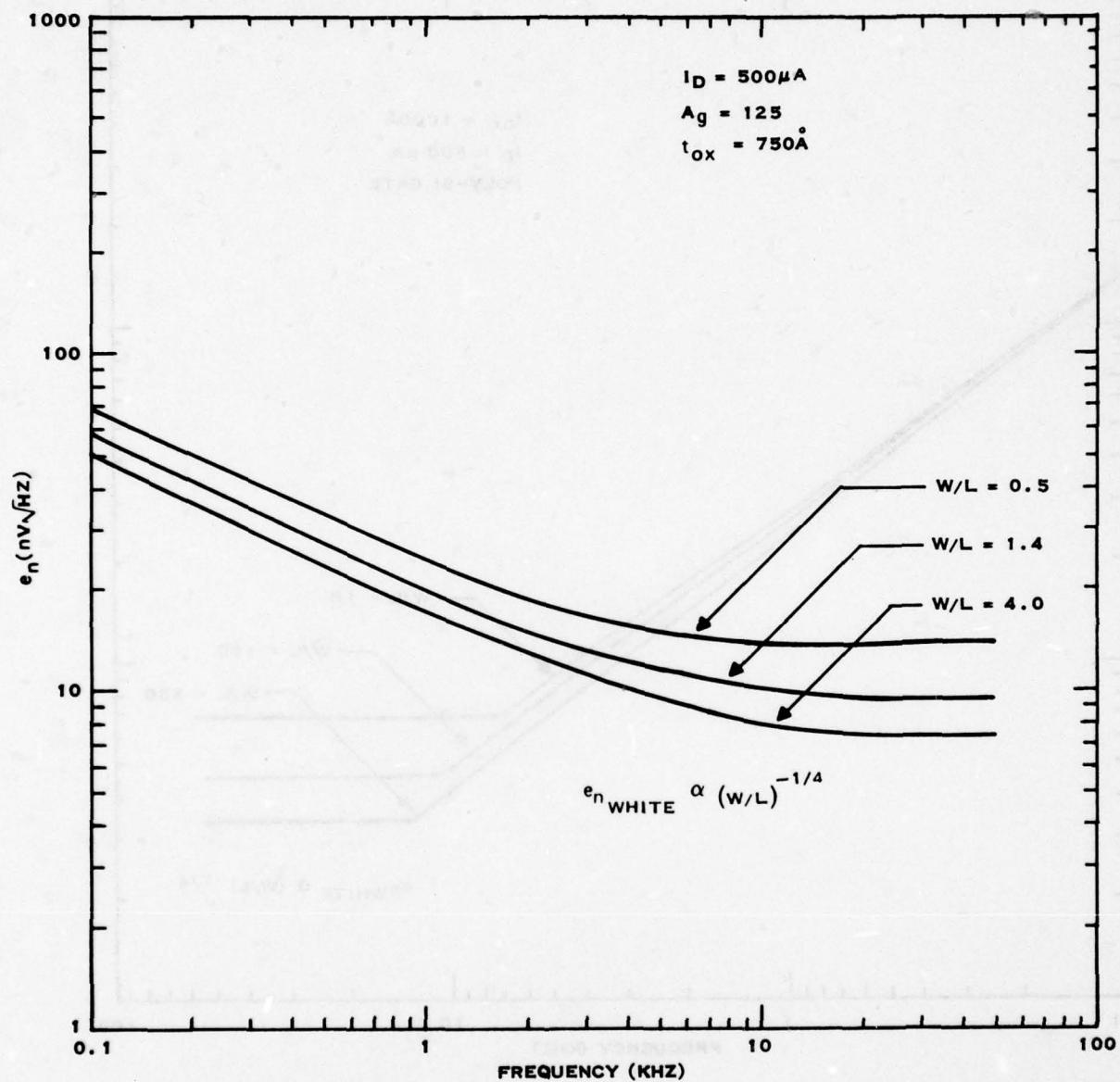


Figure 11. Surface Channel MOSFET Noise Characteristics as a Function of W/L Ratio

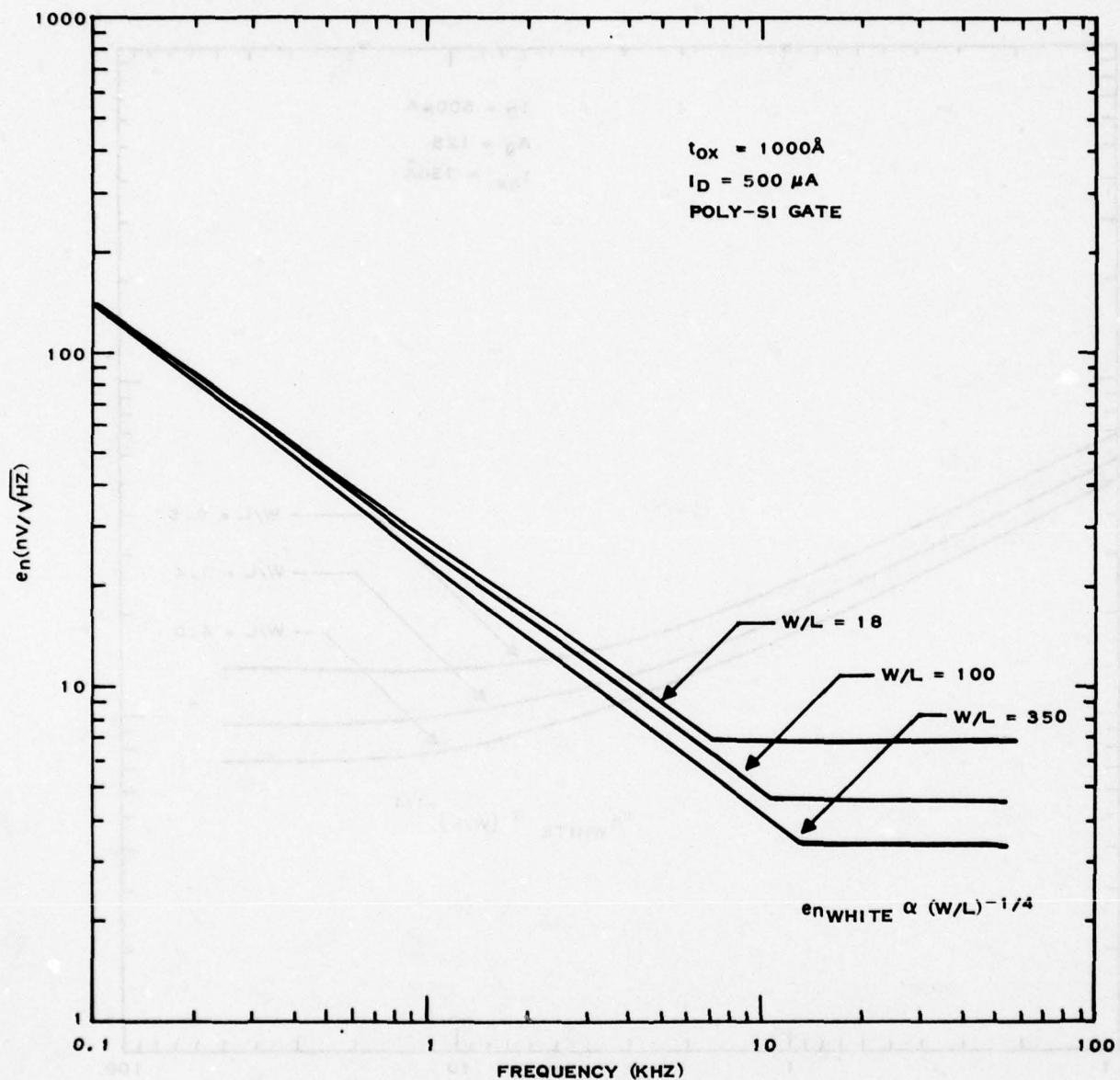


Figure 12. Buried Channel MOSFET Noise Characteristics as a Function of W/L Ratio

18 the white noise level is 7.0 nV//Hz. The fourth root of the ratio of 300 to 18 is 2.02, which compares very closely with the ratio of 7.0 to 3.5.

2. Process Parameters

The behavior in the white noise region is predicted by theory, in that g_m is increased with thinner gate oxides. Figure 13 illustrates a decrease in white noise as the gate oxide thickness is decreased from 1500 Å to 500 Å. The data for the 1500 Å gate oxide thickness were taken from a previous lot that had a small geometry device and are included to aid in establishing the functional relationship of gate oxide thickness to white noise characteristics. As with the surface channel devices, the thinner gate oxide gives a lower value of white noise and tends to follow fourth-root dependence, as shown in Figure 14. Note that the low-frequency noise is also reduced when the gate oxide thickness is reduced. The functional relationship of t_{ox} on low frequency noise is discussed in Section III.D

The minimum achievable oxide thickness is limited by pinhole density and dielectric breakdown. Neither of these mechanisms has been observed to be a major limitation with the thin (500 Å) oxides process under this contract for devices evaluated from either slice 9 or slice 10.

As discussed in Section II, the superiority of the low frequency noise performance of the buried channel MOSFET over the surface channel is the result of having the conducting channel in the bulk silicon rather than at the surface. The buried channel is implemented with an ion implantation process, and the distance that the ions diffuse into the bulk material can be controlled by the drive-in time. An objective of the experimental effort was to determine how the drive-in time affected the noise characteristics of the buried channel device. Figure 15 shows the evaluation of three buried channel MOSFETs that were identical in every respect except for the drive-in times used for the buried channel implant. Considering for the moment only the white noise

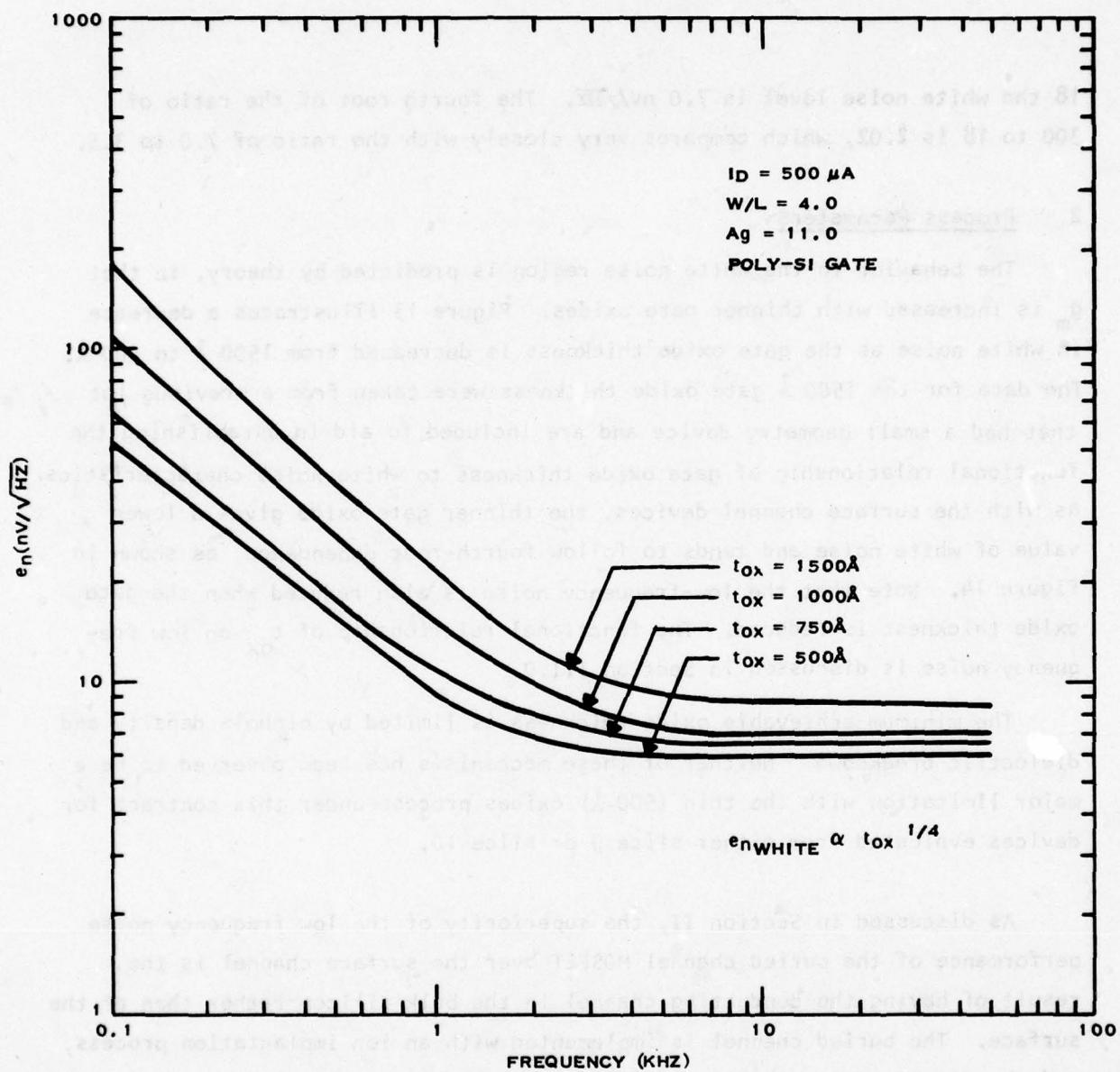


Figure 13. Buried Channel MOSFET Noise Characteristics as a Function of Gate Oxide Thickness

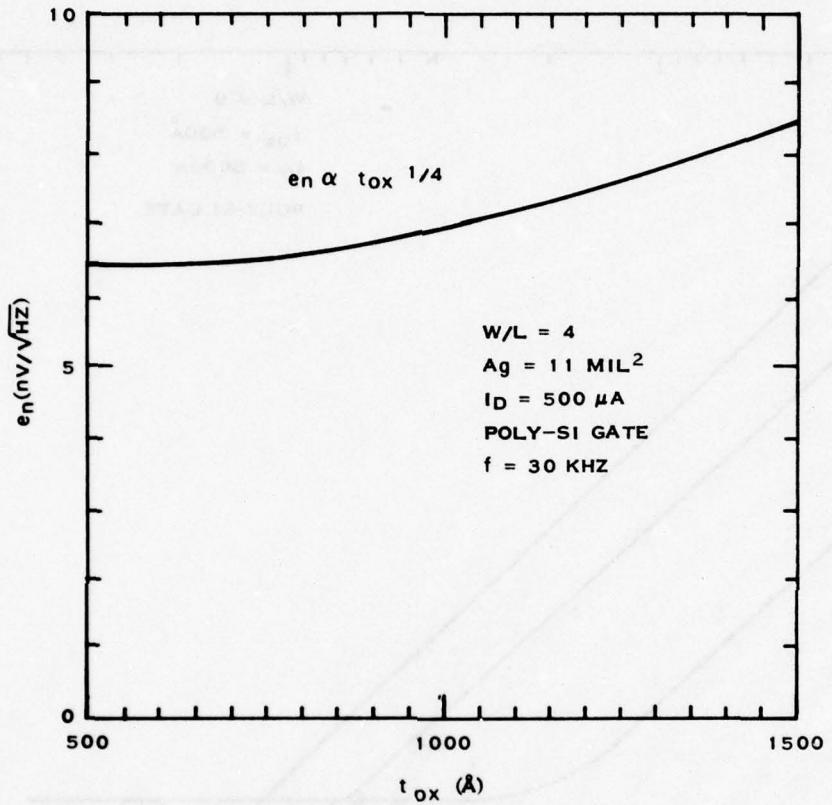


Figure 14. Buried Channel MOSFET White Noise Characteristic as a Function of Gate Oxide Thickness

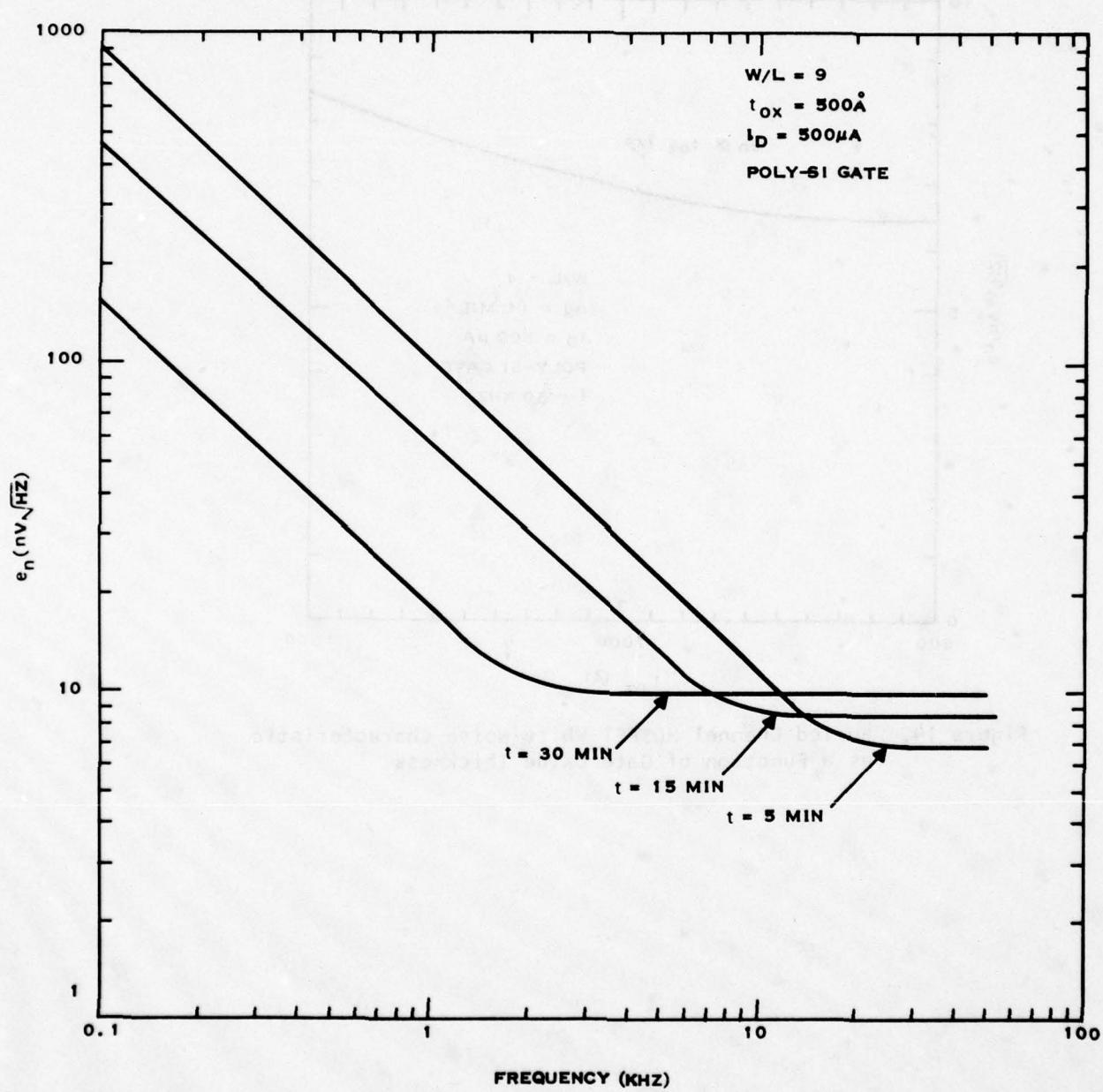


Figure 15. Buried Channel Noise Characteristics as a Function of Ion Implant Drive-In Time

region, since the low frequency region will be discussed in the next section, the white noise level decreases as the drive-in time decreases. Since the white noise level is influenced by the g_m of the device, g_m has increased because the conduction channel is closed to the gate when there is less drive-in time.

In Figure 16 the white noise is plotted as a function of drive-in time, with the noise being nearly proportional to drive-in times for the values used in this program. As shown, there is a 30% reduction in noise level from 10 nV/ $\sqrt{\text{Hz}}$ to 7 nV/ $\sqrt{\text{Hz}}$ when the drive-in time is changed from 30 minutes to 5 minutes. Hence, to obtain the lowest white noise level, the drive-in time should be minimized. However, as also shown, there is a large increase in the low frequency noise spectrum as the white noise level is decreased. Hence, there is a design trade-off between the values of noise for both the white and the low frequency region.

3. Bias Parameters

As noted in Section II, noise theory predicts an inverse fourth-root dependence on drain current for the white noise level of surface channel MOSFETs. Figure 17 gives experimental data illustrating this dependence for buried channel devices. The low frequency noise does not appear to be significantly dependent on bias level. In general, these data show that the buried channel device conforms to the well-developed theory for the surface channel MOSFET, having the same functional dependence on bias level in the white noise region and little or no dependence in the low frequency region.

Buried channel MOSFET noise characteristics were evaluated with respect to temperature over a range from -50°C to 70°C . Surface channel MOSFET theory predicts decrease in white noise with decreasing temperature after the following relationship:

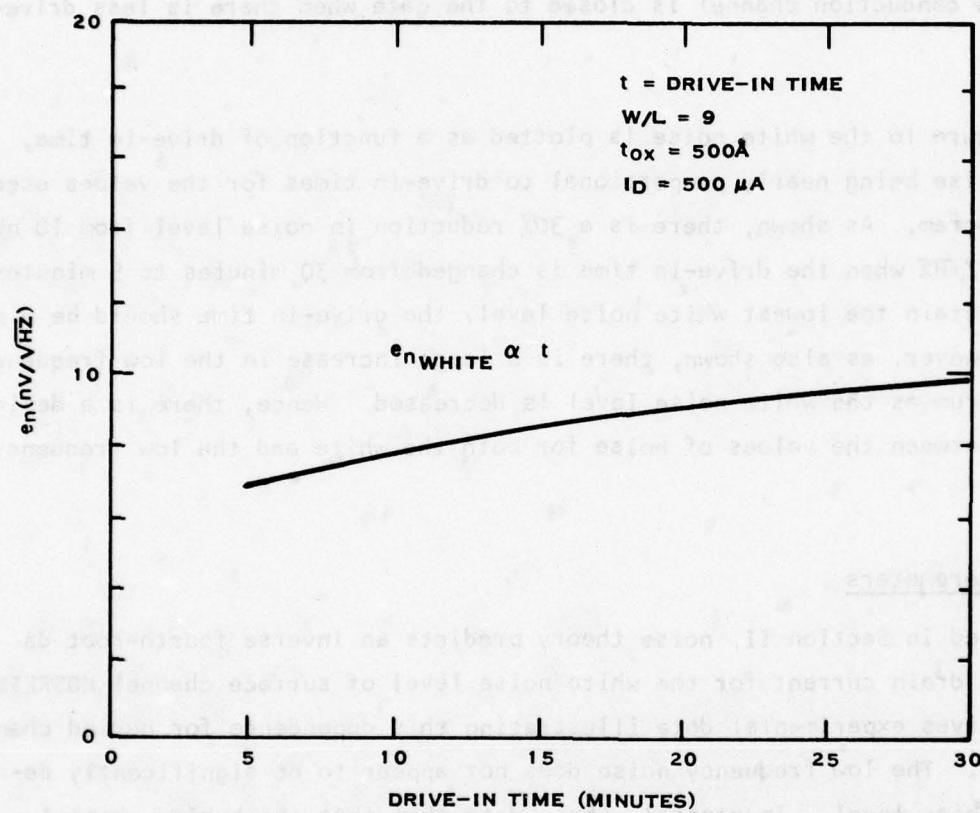


Figure 16. Buried Channel White Noise As a Function of Drive-In Time

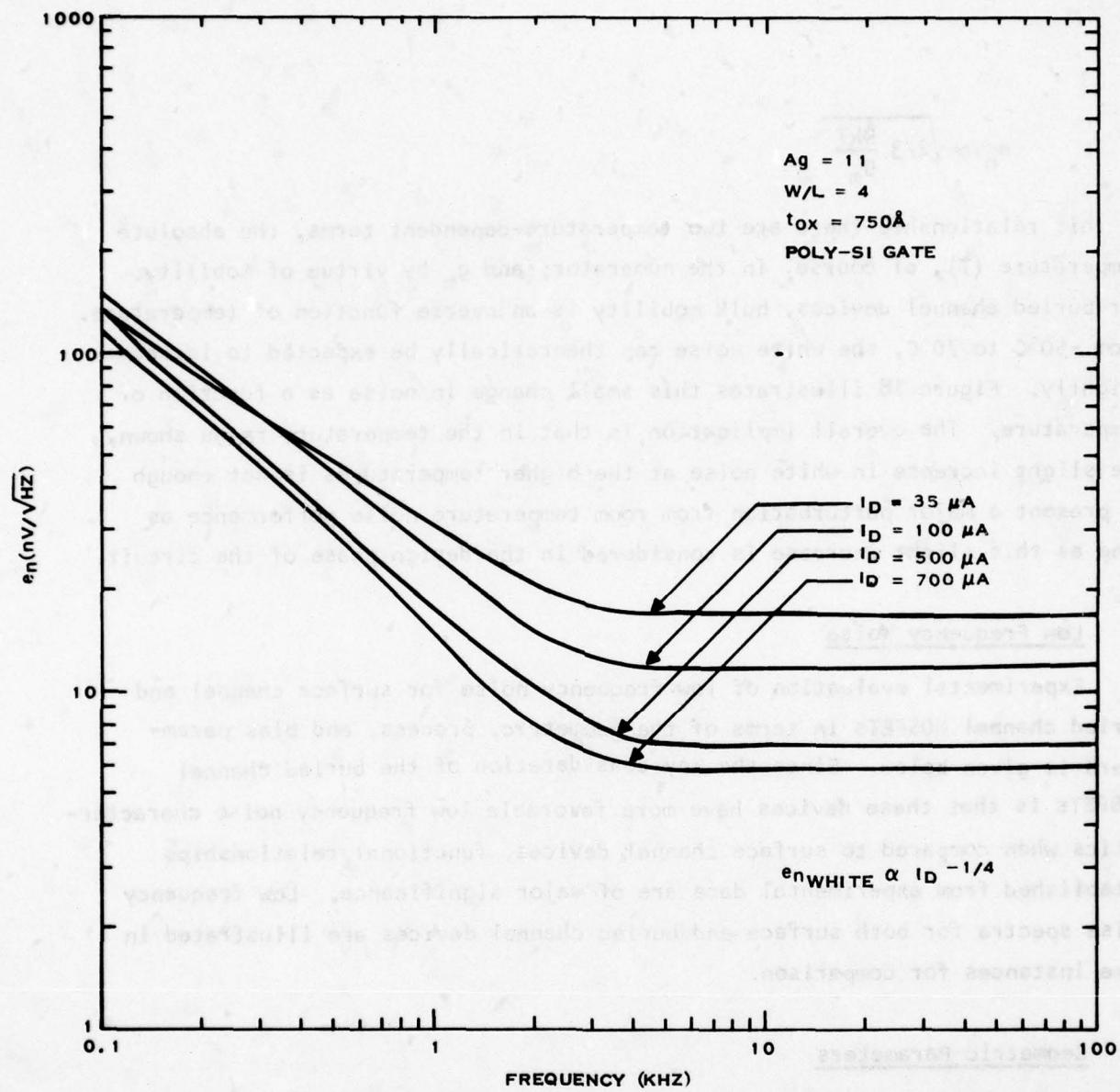


Figure 17. Buried Channel MOSFET Noise Characteristics as a Function of Drain Current

$$e_n \approx \sqrt{2/3} \frac{4kT}{g_m}$$

In this relationship there are two temperature-dependent terms, the absolute temperature (T), of course, in the numerator; and g_m by virtue of mobility. For buried channel devices, bulk mobility is an inverse function of temperature. From -50°C to 70°C, the white noise can theoretically be expected to increase slightly. Figure 18 illustrates this small change in noise as a function of temperature. The overall implication is that in the temperature range shown, the slight increase in white noise at the higher temperatures is not enough to present a major perturbation from room temperature noise performance as long as this slight increase is considered in the design phase of the circuit.

D. Low Frequency Noise

Experimental evaluation of low frequency noise for surface channel and buried channel MOSFETs in terms of the geometric, process, and bias parameters is given below. Since the key consideration of the buried channel MOSFETs is that these devices have more favorable low frequency noise characteristics when compared to surface channel devices, functional relationships established from experimental data are of major significance. Low frequency noise spectra for both surface and buried channel devices are illustrated in some instances for comparison.

1. Geometric Parameters

Figure 19 illustrates a surface channel MOSFET noise spectrum as a function of gate area, A_g . The W/L ratio is 4, and the gate areas are 0.28 and 3.18 mm^2 (11 and 125 mils 2). Considering the relationship between these two surface channel devices in the low frequency region, the level of 1/f noise is seen to shift as the gate area is decreased. This varies approximately with the inverse square root relationship predicted by theory (Section II). White noise is not dependent on gate area in these devices, although this is not apparent from Figure 19, since the smaller gate area surface channel device

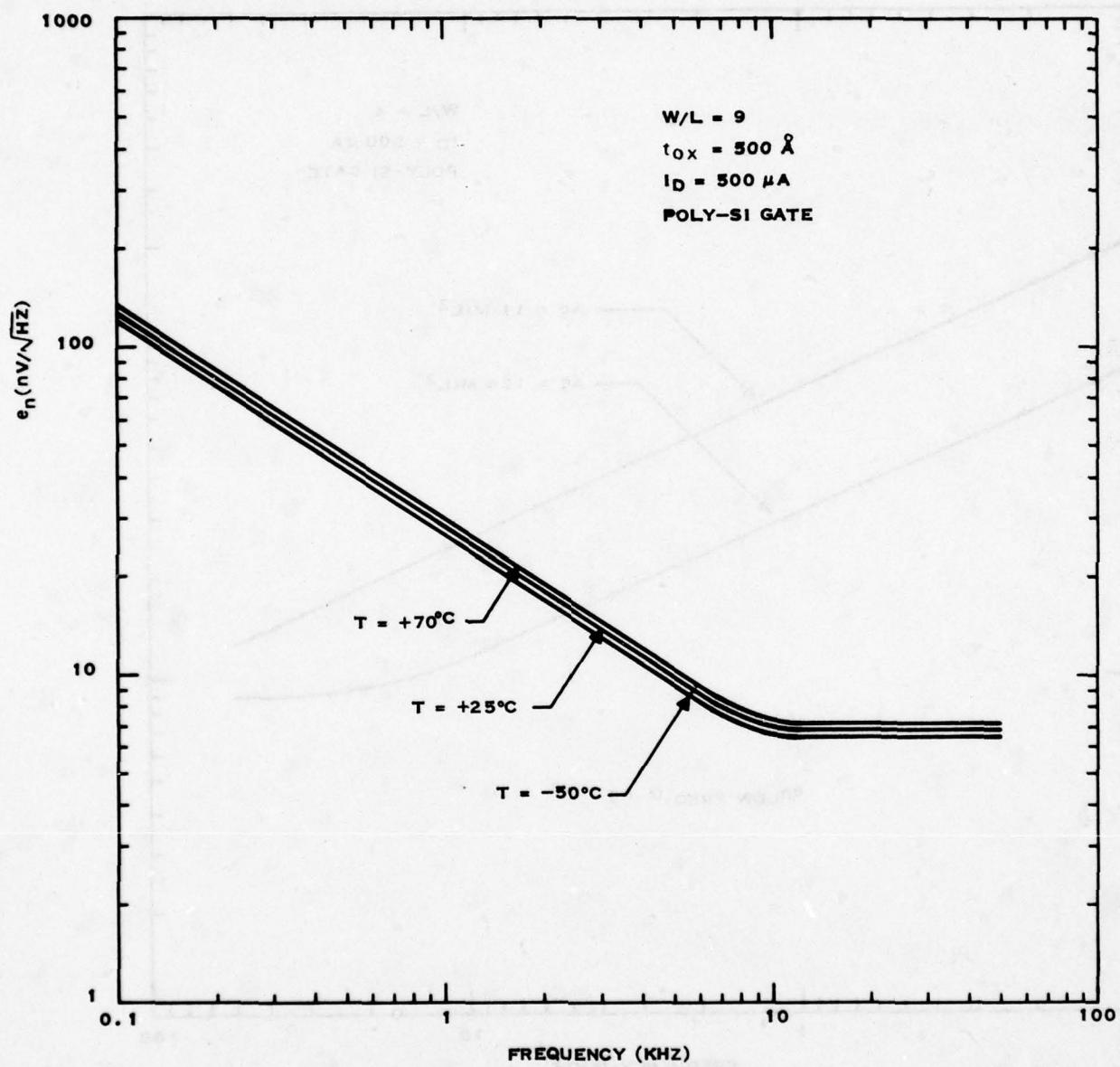


Figure 18. Buried Channel MOSFET Noise Characteristics as a Function of Temperature

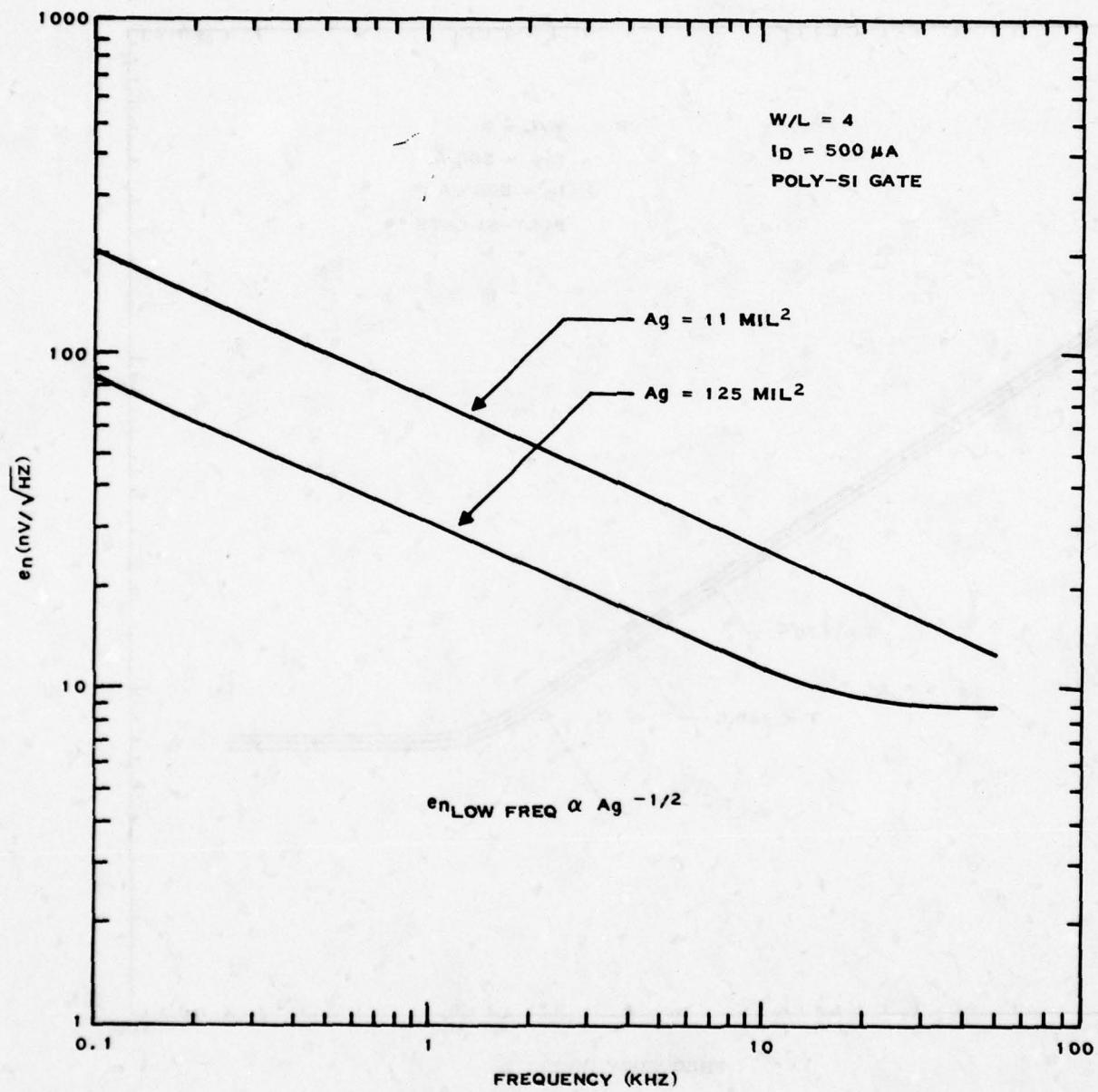


Figure 19. Surface Channel MOSFET Noise as a Function of Gate Area

has a $1/f$ corner beyond the range of measurement. However, this theory has been verified with other surface channel devices.

The low frequency noise in the buried channel device as a function of gate area has a functional relationship similar to that of the surface channel devices. As shown in Figure 20, gate area is varied from 0.15 mm^2 to 2.5 mm^2 (6 mil^2 to 100 mil^2), and the low frequency changes average close to those of low frequency surface channel MOSFET theory. The apparent decrease in white noise level, as a function of gate area as shown, is not predicted by theory and should be considered a slight anomaly, since this relationship did not appear to be correlated with other measurements.

The experimentally observed low frequency noise on large interdigitated W/L devices was considerably greater than expected. This is illustrated in Figure 21. Also note that the slope of the low frequency noise spectrum is more like $1/f$ noise than the typical g-r noise behavior. Several theories concerning this anomalous behavior have been considered, but the most credible one relates to the device layout. The large W/L devices for both the preamplifier and test structures were configured with source-drain diffusions that are interdigitated as shown in Figure 22. Large surface channel devices have been designed using this method to avoid unusually long, slender geometries, and the extension to buried channel devices was therefore logical. The cause of this increase in low frequency noise is postulated to be within the channel around the diffused fingers of the source and drain. Ordinarily, in surface channel devices the increased electric field intensity at the corners of the diffusions would not exceed the avalanche breakdown field strength. However, with the increased doping level of the buried channel and residual lattice damage inherent in the implantation process, localized avalanching could be occurring in the corner regions, causing a large increase in low frequency noise. This theory has been verified somewhat with preliminary test results on long, linear in-line test devices, where low frequency noise was considerably lower as shown in Figure 21. Future device layouts should consist of linear in-line or

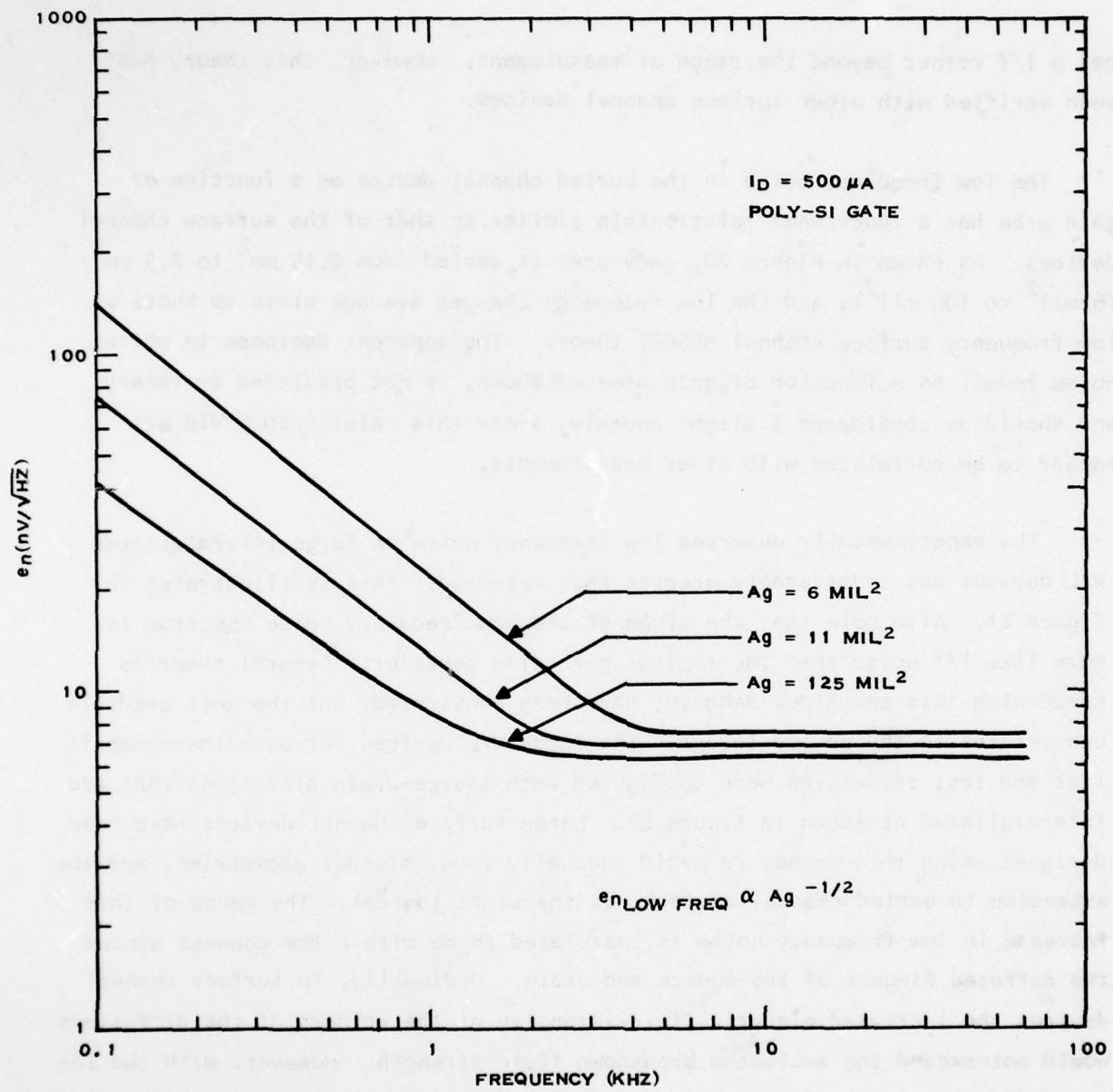


Figure 20. Buried Channel MOSFET Noise Characteristics as a Function of Gate Area

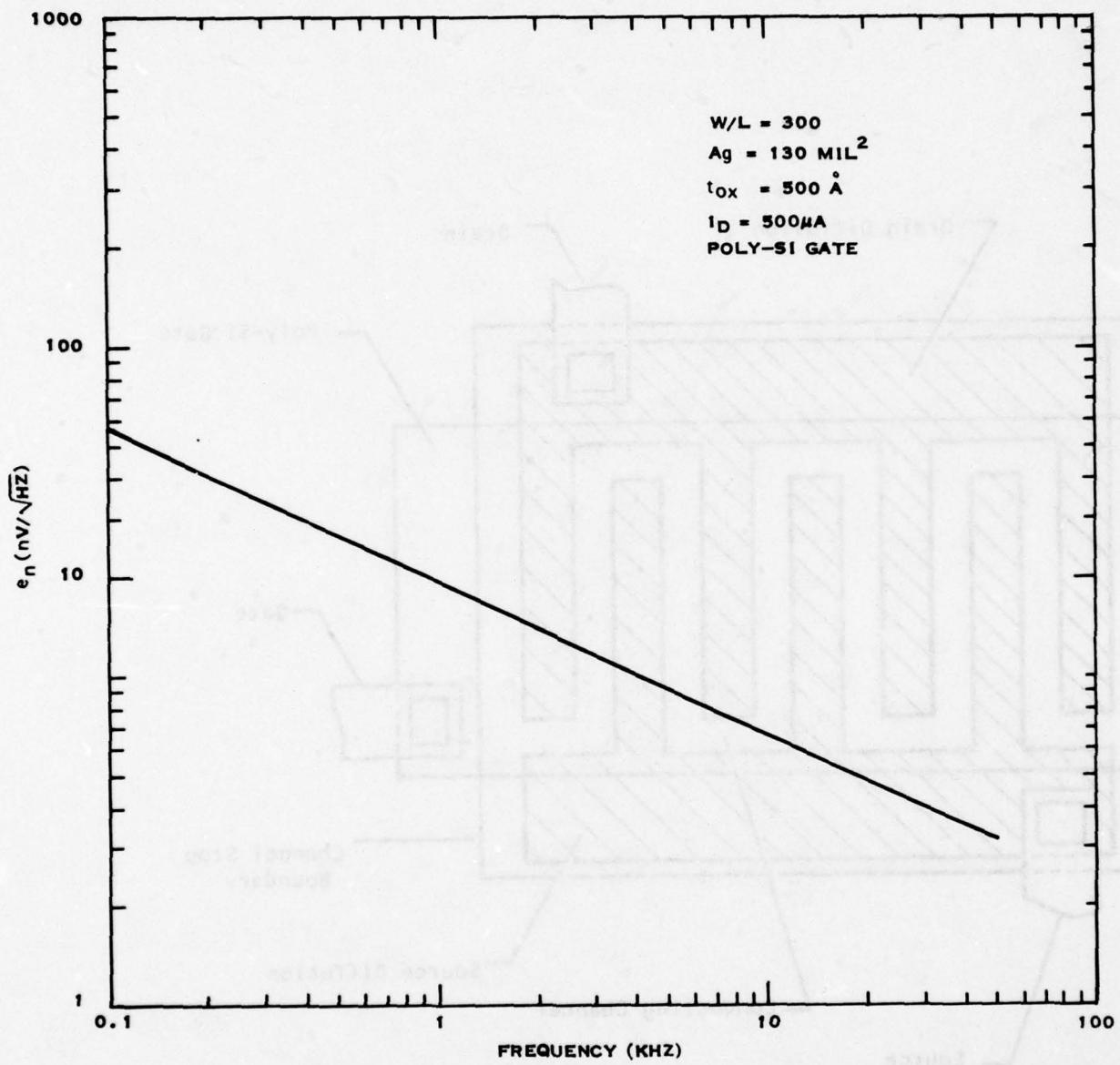


Figure 21. Noise Characteristic of Interdigitated Buried Channel MOSFET Used in the First Stage of the Preamplifier

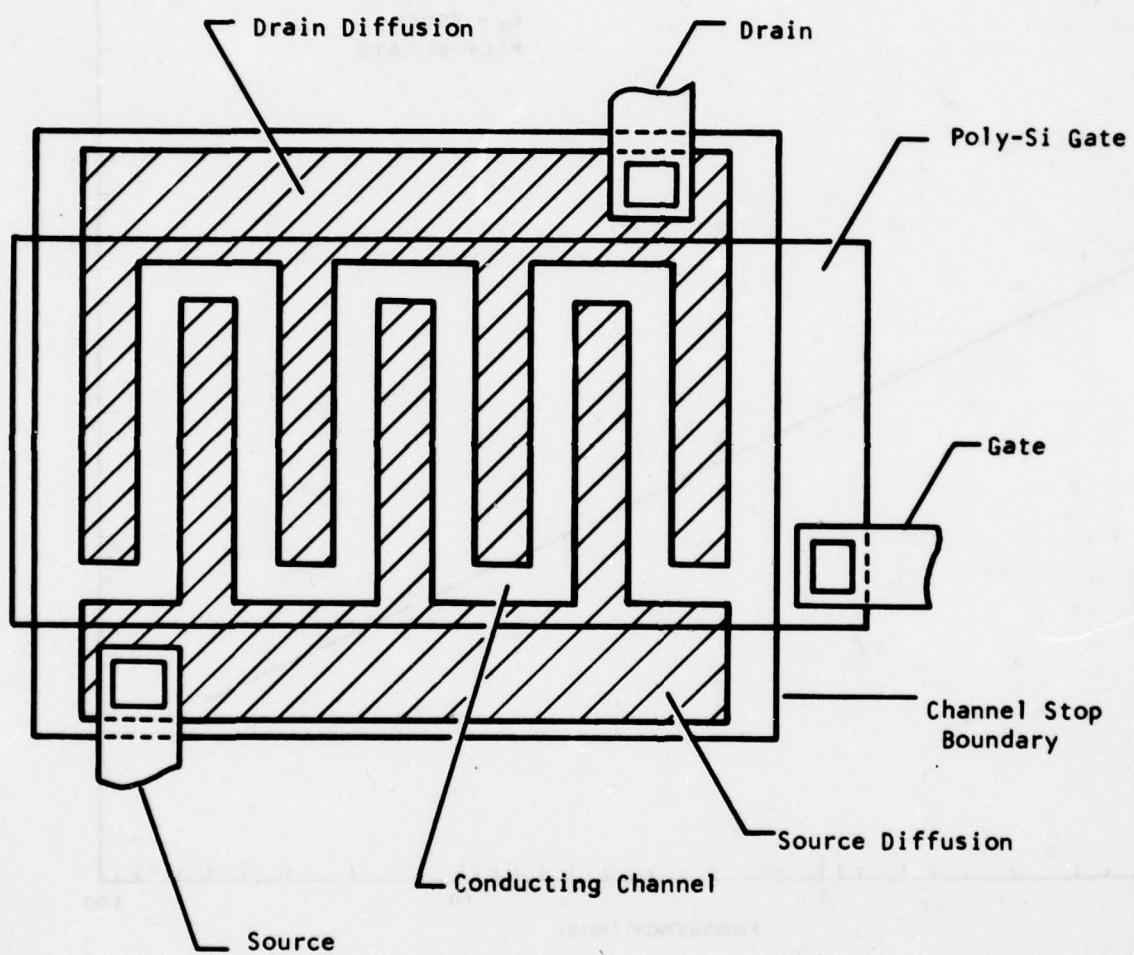


Figure 22. Interdigitated MOSFET Layout

serpentine buried channel MOSFETs, as shown in Figure 23, to avoid such problems. Furthermore, a technique could also be used whereby the sharp right-angle corners of the source-drain diffusions could be eliminated by rounding if an interdigitated configuration is required.

2. Process Parameters

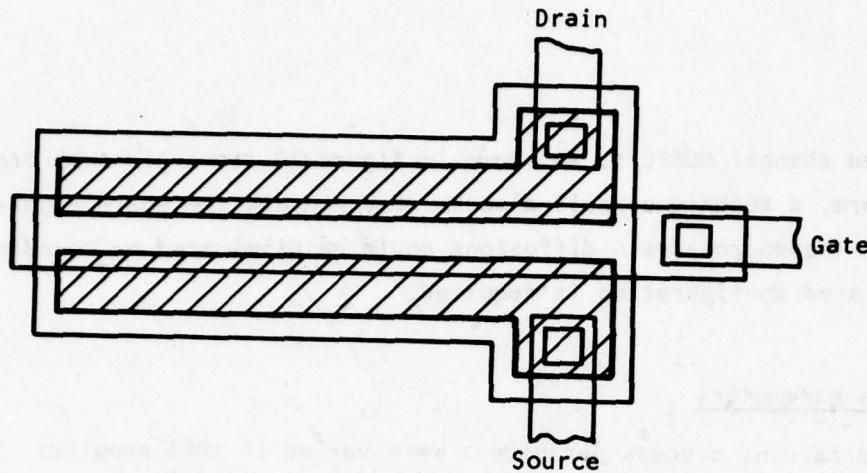
Three different process parameters were varied in this program: the gate oxide thickness, ion implant drive-in time, and gate material. Gate oxide influence on low frequency noise is discussed below, followed by discussions of ion implant drive-in time and gate material.

Figure 13 showed the noise spectrum of a buried channel MOSFET as a function of gate oxide thickness. From this figure, a curve is generated for a constant frequency ($f = 1$ kHz) to illustrate the experimentally observed functional dependence of low frequency noise on gate oxide thickness. This relationship is shown in Figure 24 and tends to be in the range of

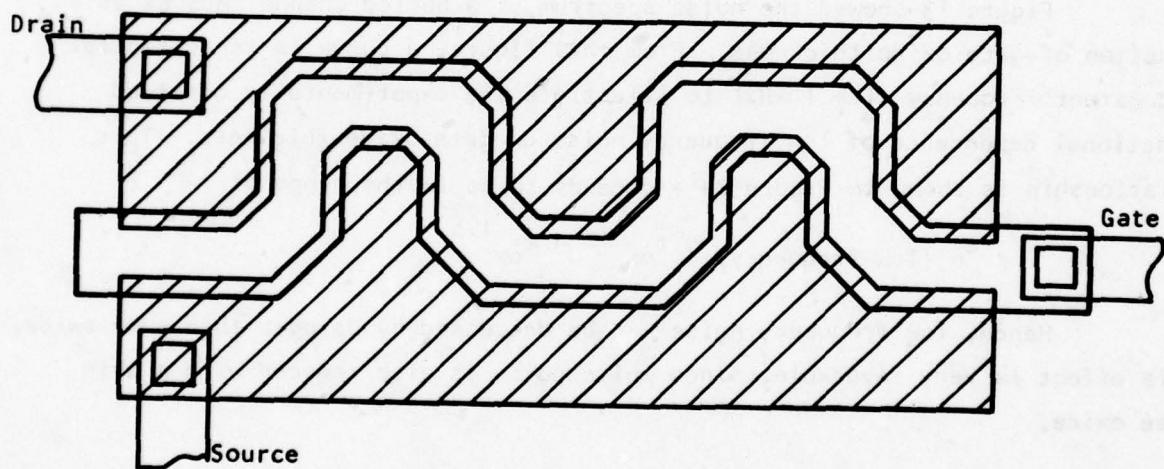
$$e_n \text{ (low-frequency)} \propto t_{ox}^{1.2} \rightarrow t_{ox}^{1.5}$$

Hence, low frequency noise can be decreased by using a thin gate oxide. This effect is very favorable, since white noise is also reduced with a thin gate oxide.

Experimental results have shown (see Figure 15) that implant depth is an important parameter in fabricating buried channel MOSFETs with good low frequency noise performance. Data from this figure are used in Figure 25. As shown, the low frequency noise level at a frequency of 1 kHz decreases from 100 nV/ $\sqrt{\text{Hz}}$ for a 5 minute drive-in time to 17 nV/ $\sqrt{\text{Hz}}$ for a drive-in time of 30 minutes. This is more than fivefold decrease in low frequency noise. Considering the shift between the 15 minute and 30 minute points of this figure, it is likely that a further decrease in low frequency noise could be obtained for longer drive-in time of, e.g., 45 or 60 minutes.



(a) Linear In-Line



(b) Serpentine

Figure 23. Linear In-Line and Serpentine MOSFET Layouts

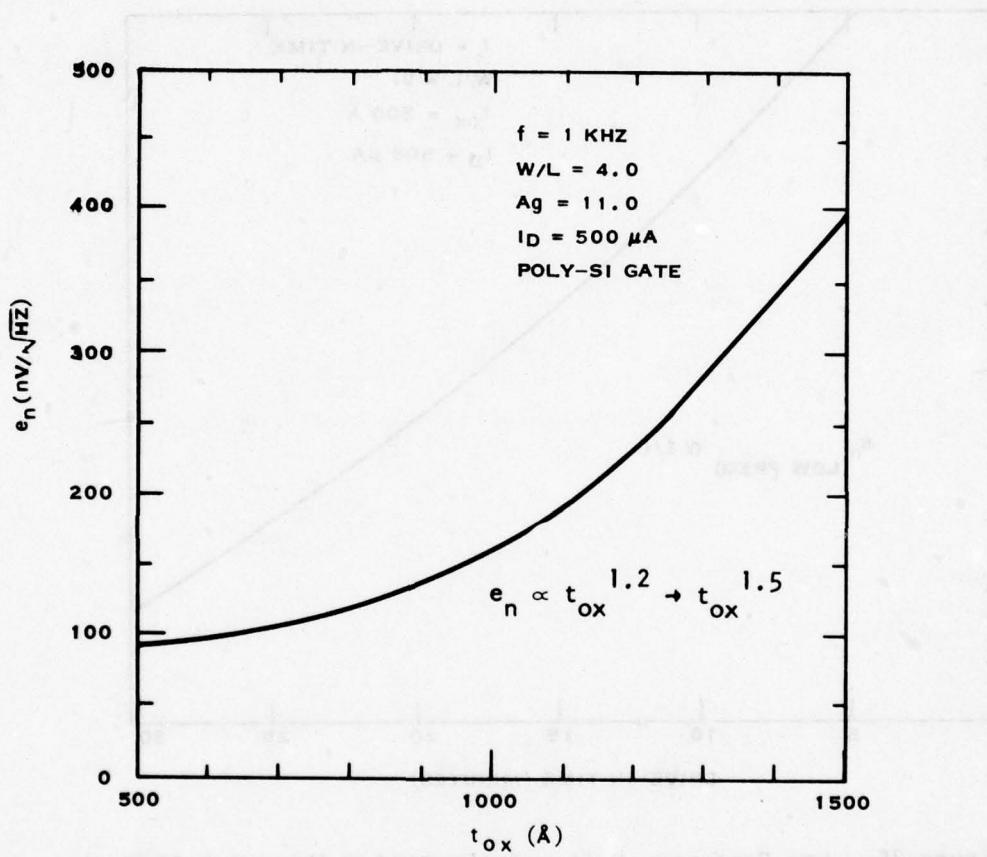


Figure 24. Buried Channel MOSFET Low Frequency Noise Characteristics as a Function of Gate Oxide Thickness

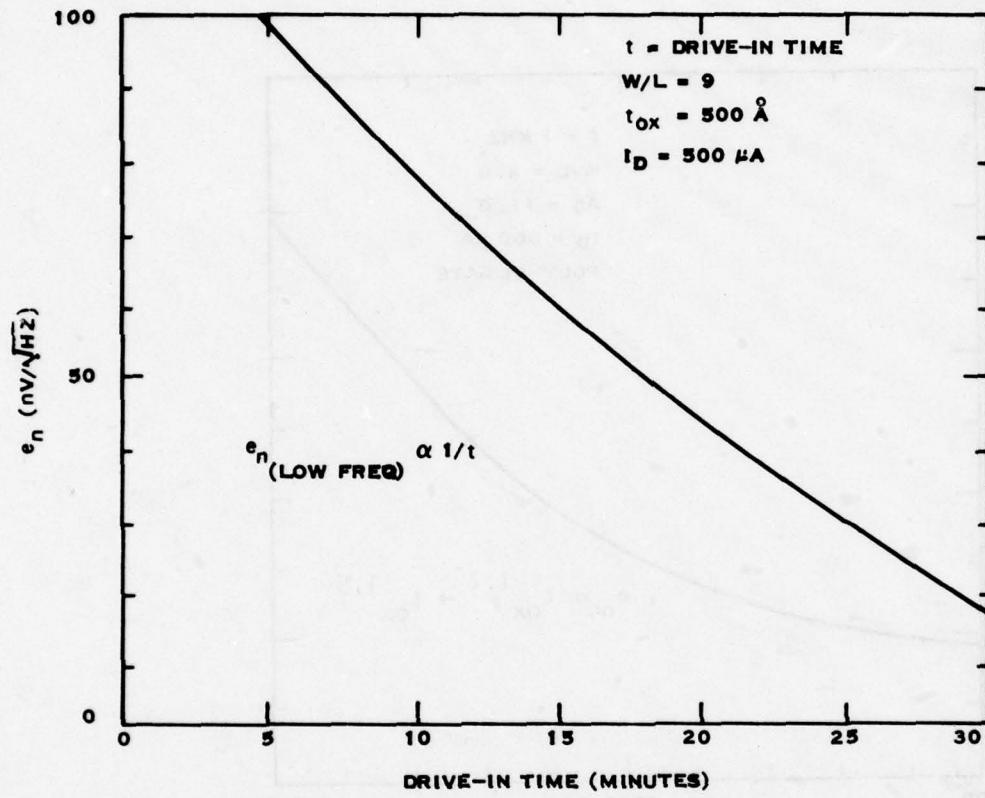


Figure 25. Low Frequency Noise of the Buried Channel MOSFET as a Function of Implant Drive-In Time

Note from Figure 15 that as low frequency noise decreases, there is an increase in white noise level. A close form functional relationship has not been determined for low frequency noise as a function of drive-in time, but Figure 25 suggests that there is a nearly linear relationship between low frequency noise and ion implant drive-in time for the values shown.

As noted, when the ion implant drive-in time increases, the low frequency noise decreases. However, in some applications voltage bias problems may be encountered due to the larger negative threshold voltages and substrate voltage bias required with deep implant channel devices. This is significant in applications where it is desirable that the substrate be held at ground potential. In other applications where a very low white noise level is required, below 5 or 6 nV/ $\sqrt{\text{Hz}}$, for example, the deep implant device may require large values of both drain current and gate area. Under these conditions, a shallower implant may be attractive, with the low frequency noise levels regained by increasing the device gate area.

The reduction in low frequency noise results from the use of polysilicon as a gate material instead of aluminum (Figure 26). As indicated, nearly an order of magnitude of improvement in reduction of low frequency noise occurs when the polysilicon gate structure is used. Although the exact noise mechanism was not defined in this effort, experimental evidence strongly indicates that polysilicon gate structures are superior to aluminum.

3. Bias Parameters

The effect of bias parameters on low frequency buried channel MOSFET noise characteristics was evaluated. No significant dependence on bias parameters was expected in the buried channel devices with regard to low frequency noise characteristics. In surface channel MOSFETs there is a low frequency noise dependence on gate voltage. This dependence is related to the effect of gate voltage on surface states. The buried channel device noise was measured

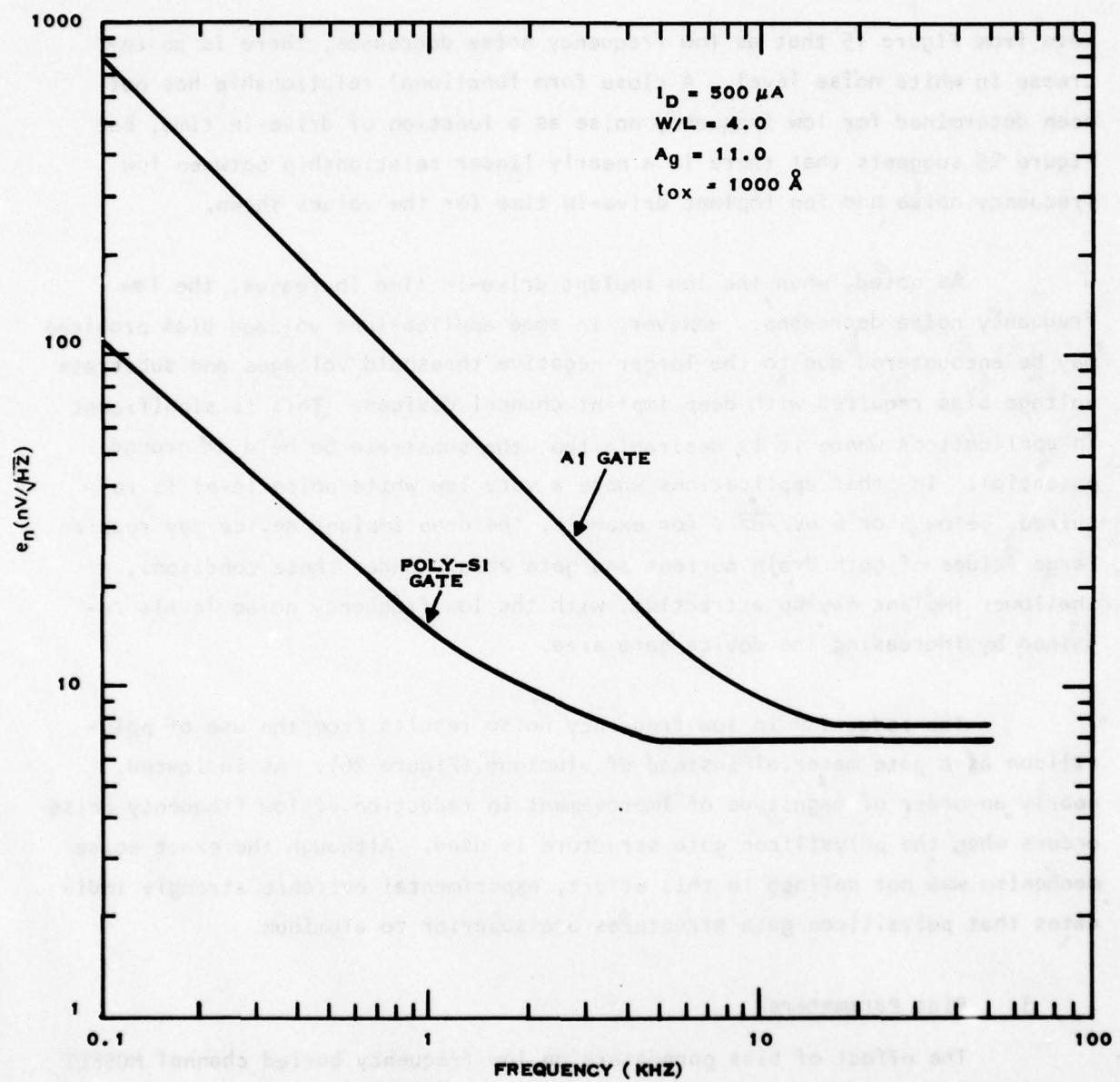


Figure 26. Buried Channel Poly-Si and Aluminum Gate MOSFET Noise Characteristics

as a function of gate voltage; the results showed little dependence in the low frequency region.

The temperature effect on low frequency noise is shown in Figure 18. As indicated for the temperature range shown, there is only a slight change in low frequency noise as a function of temperature.

E. Summary of Buried Channel MOSFET Experimental Results

Functional relationships are established in this section to describe the dependence of buried channel MOSFET noise performance on geometric, processing, and bias parameters. These relationships are useful as guidelines in designs of buried channel MOS preamplifier circuits for optimum low noise performance while maintaining CCD process compatibility. Table 3 summarizes the dependence of these parameters on the buried channel MOSFET noise characteristics. The noise spectrum is affected by the geometric parameters through W/L ratio as the inverse fourth root in the white noise region and for the low frequency noise region by the inverse square root function. The process parameters t_{ox} and ion implant drive-in time modify the noise spectrum as indicated. The polysilicon gate structure was found to have a lower noise corner than the aluminum gate device. Bias parameters have a much weaker influence on the buried channel MOSFET than do geometry and process parameters. As discussed in Section III.D, the large interdigitated MOSFETs were observed to have much higher than expected low frequency noise levels. This discrepancy is explained and a solution presented.

TABLE 3
BURIED CHANNEL MOSFET NOISE CHARACTERISTICS
AS A FUNCTION OF THE GENERALIZED PARAMETERS

| <u>Parameter</u> | <u>White</u> | <u>Low Frequency</u> |
|------------------------------|-------------------------|---|
| Geometric - W/L | $(W/L)^{-\frac{1}{4}}$ | $A_g^{-\frac{1}{2}}$ |
| - Gate area, A_g | | |
| Process - t_{ox} | $t_{ox}^{-\frac{1}{4}}$ | $t_{ox}^{1.2} \rightarrow t_{ox}^{1.5}$ |
| - Implant Drive-in Time, t | t | t^{-1} |
| - Gate material | | Poly-Si < Al |
| Bias - I_D | $(I_D)^{-\frac{1}{4}}$ | |

SECTION IV
BURIED CHANNEL MOS PREAMPLIFIER DESIGN AND EVALUATION

A. Buried Channel Preamplifier Design

The low noise buried channel MOS preamplifier design goal was to have a gain of 75 with an input equivalent white noise voltage of 4 nV/ Hz and a low frequency corner at 1 kHz. Large geometry buried channel devices were used in the two gain stages to ensure the best possible low noise performance. To achieve desired gain and frequency stability as well as gain matching between preamplifiers as required in a parallel image buffer system, negative feedback was employed using resistive ratios to set the closed loop characteristics. Overall process compatibility with the image buffer was considered throughout the design of the preamplifier.

The buried channel MOS preamplifier configuration is shown in Figure 27. Basically, the preamplifier design utilizes two cascaded buried channel MOSFET inverter stages with depletion-type active loads. A source-follower output buffer is used to drive the output load in addition to providing series feedback to the first amplifier stage. The input device, M2, is a large interdigitated buried channel structure with noise characteristics determining the overall preamplifier noise performance, since significant gain occurs in the first stage. The device was designed to have a theoretical white noise of 4 nV/ Hz and a low-frequency corner of 1 kHz with a W/L ratio of 300 and I_D of 1 mA. The load device of the first stage, M1, is also a buried channel with the gate tied to the source, providing a high series resistance typical of depletion load devices. The design gain of this stage is approximately 40.

The second stage amplifier has a design noise of 6 nV/ Hz ; thus, when referred to the input of the preamplifier, it is a negligible contributor to the total noise. The second inverter gain stage consisting of M3 with a W/L ratio of 0.2 and M4 with a W/L ratio of 10 provides additional open loop gain and, in conjunction with C_C , provides internal closed loop frequency compensation and bandwidth control. The final stage of the preamplifier is a

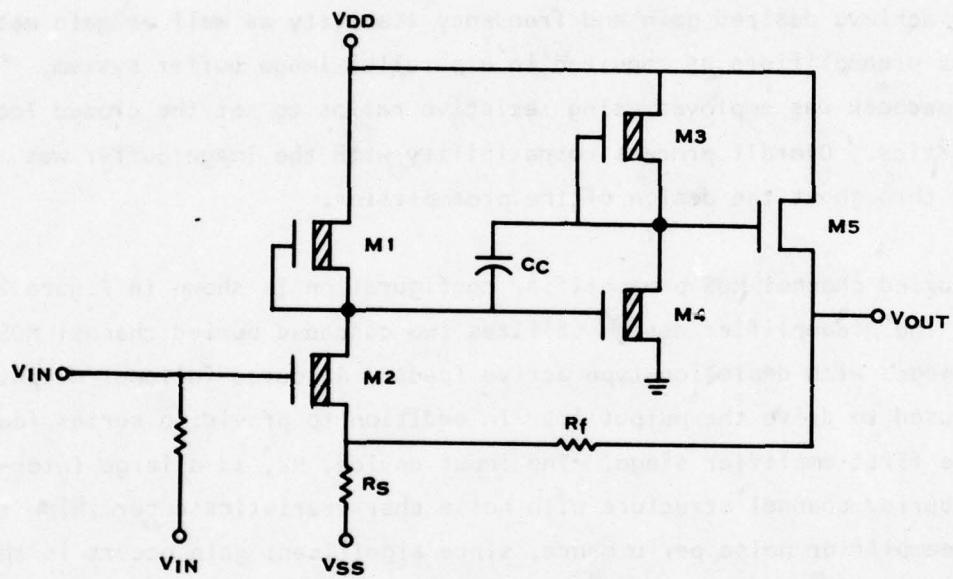


Figure 27. Buried Channel Low Noise MOS Preamplifier

surface channel source-follower stage which buffers the amplifier output stage for the output load and feedback and reduces the power dissipation in the feedback network. In addition to stabilizing the ac characteristics, the feedback arrangement also stabilizes dc characteristics within the loop, which is particularly important in terms of MOSFET threshold voltage variations. A computer-aided design program indicates the ac gain is approximately 75 and is controlled by the feedback network. Critical bias voltages must still be supplied at the gate of M2, and the V_{ss} supply must be well regulated and "quiet." As discussed in Section III, to achieve proper operation of the large W/L MOSFETs, substrate bias must be applied to the substrate. The design value of substrate voltage is -5.0 V.

The feedback resistors R_f and R_s are implanted structures fabricated with the buried channel ion implant. Sheet resistivities are on the order of $5 \text{ k}\Omega/\text{square}$ and provide adequate linearity for this application. Although developed in the initial phase of this effort, the special linearized MOSFET resistor-pairs (see the appendix) were unnecessary for this design, since MOSFET M5 drops most of V_{DD} , and small signal operation imposes only small voltage variation on the feedback resistor R_f . The closed loop gain is dependent only on the ratio of these resistances, so absolute values are noncritical so long as adequate bias can be maintained at the source of M2. A computer-aided-design dc analysis program indicated linear operation over a $\pm 2 \text{ V}$ range at the output. Assuming a gain of 75 and a white noise of $1 \mu\text{V}$ yields a predicted dynamic range of $> 80 \text{ dB}$. The buried channel preamplifier is designed to have a drain current of 1 mA for the first stage. The design goal for chip area for the preamplifier was to be less than 25.4 mm^2 (1000 mil^2) and was less than 20.3 mm^2 (800 mil^2) in the final layout.

B. Preamplifier Experimental Results

The purpose of this section is to discuss the performance of the low noise buried channel MOS preamplifier. The overall dc and ac characteristics of this

design are excellent. However, the low frequency noise contributed by the interdigitated structure used in the first stage is excessive. As discussed in Section III.D, this type of device structure yields a much larger value of low frequency noise as a result of the interdigitated structure. In subsequent buried channel design, this problem can be eliminated and a low corner frequency of 1 kHz should be obtainable. The preamplifier was evaluated for the following performance parameters:

- 1) Gain/bandwidth
- 2) Input noise characteristics
- 3) Dynamic range and linearity
- 4) Power dissipation
- 5) Bias effects
- 6) Temperature effects.

Preamplifiers from several different slices, each of which had processing variations on implant depth and gate oxide thickness (see Section III.B), were evaluated. Each preamplifier was tested in the configuration shown in Figure 28 at the supply levels indicated. Values of V_{ss} and V_{GS} were adjusted to compensate for processing variations from slice to slice unless otherwise stated.

1. Gain/Bandwidth

The gain and bandwidth design goal for the preamplifiers from four different slices are shown in Figure 29. Each preamplifier was tested using an HP3510A wave analyzer with the tracking generator supplying the sweep frequency input. For this evaluation, the test box was biased for a given preamplifier and was unchanged for the other three preamplifiers. Gain ranged from 31.2 dB to 37.2 dB with a bandwidth of 40 to 70 kHz. Gain variation occurs because the individual preamplifiers operate slightly out of the optimum dc bias region, since rather large processing variations were imposed (i.e., oxide

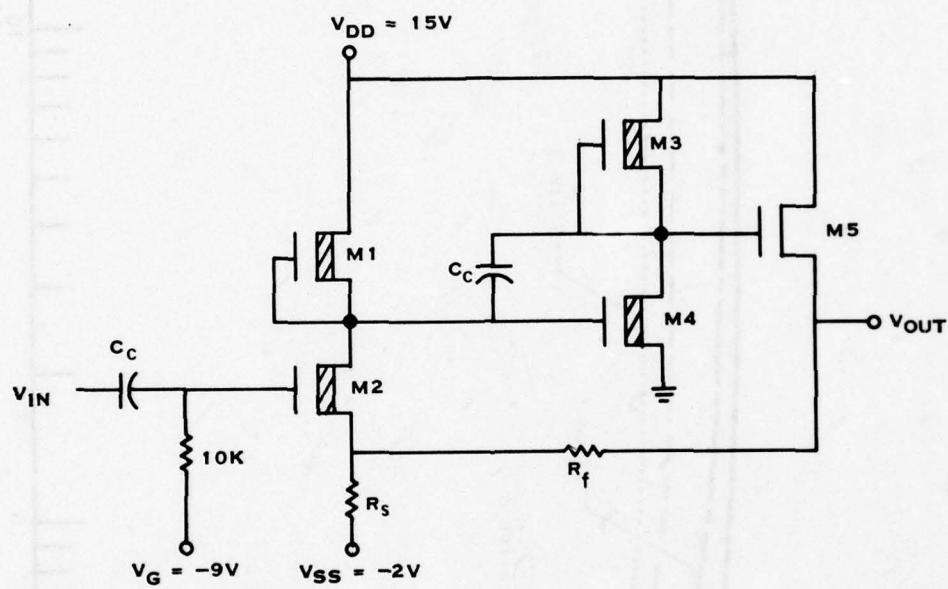


Figure 28. Preamplifier Bias Levels

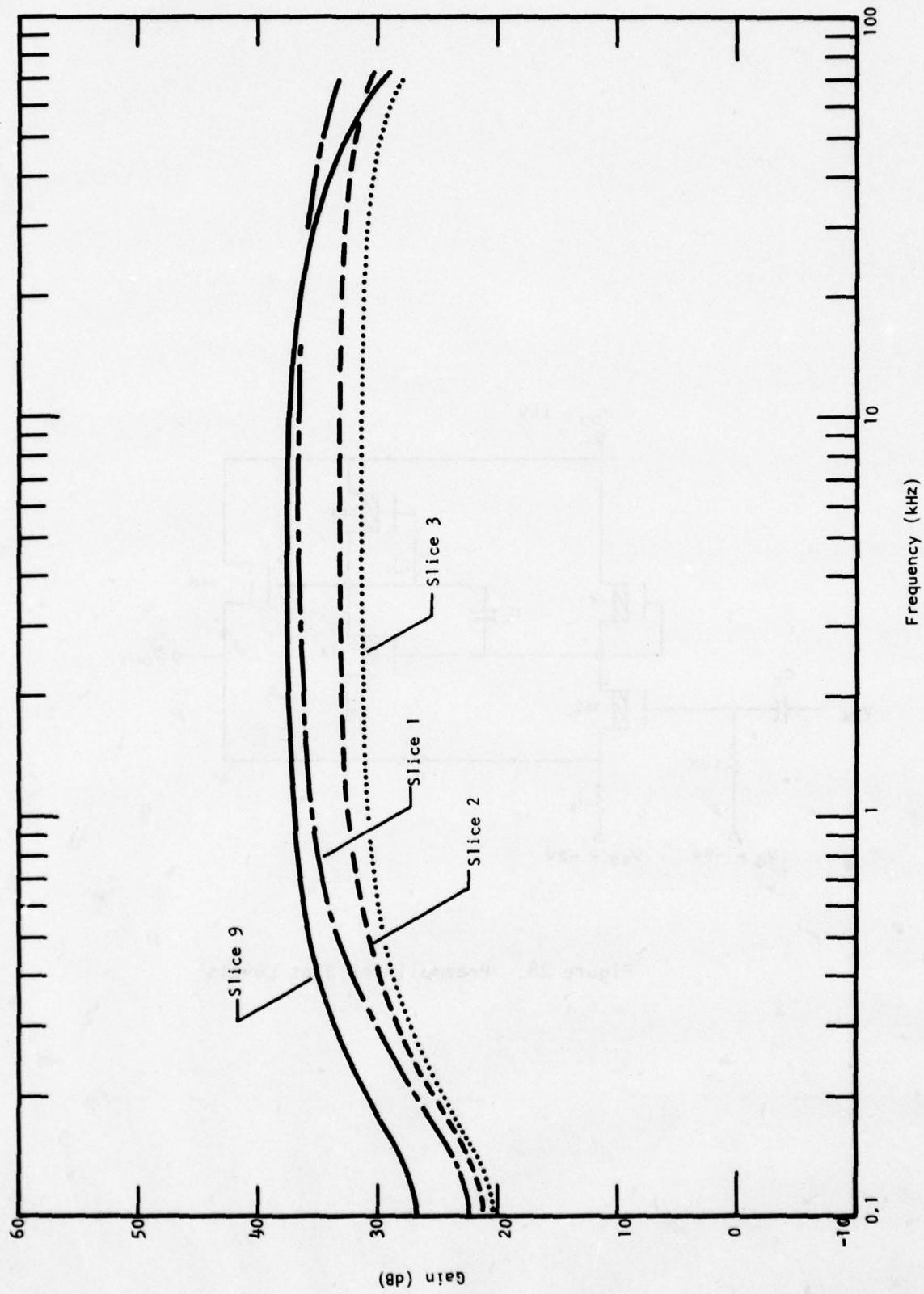


Figure 29. Gain of Buried Channel Preamplifiers

thickness and implant depth). The fact that the preamplifiers were all operable at the same bias point, however, indicates the good closed loop dc characteristics of the feedback preamplifier. Hence, for a given set of process parameters, the above design gain and bandwidth goals should be obtainable in later designs.

2. Input Noise

The input noise characteristics of the preamplifier were measured using an HP3510A wave analyzer as shown in Figure 30. Several measurements of preamplifiers with varying implants and oxide thicknesses were made, and Figure 31 shows the typical achievable noise level in the tests. Again, the low frequency noise corner is extended beyond the design goal of 1 kHz, because the input device is an interdigitated MOSFET. The discussion in Section III.D on low frequency noise of interdigitated devices applies here also, since the large input buried channel device is the dominant noise source of the preamplifier. In future designs this problem can be eliminated by using noninterdigitated MOSFETs in the first gain stage of the preamplifier. Nevertheless, the design goal of $4 \text{ nV}/\sqrt{\text{Hz}}$ for the white noise region should be reached even for interdigitated structures. However, Figure 31 shows that there is rise in the white noise spectrum of the preamplifier equivalent input noise. As shown, the lowest value of white noise is $6 \text{ nV}/\sqrt{\text{Hz}}$. This increase in the white noise is due to preamplifier internal gain frequency roll-off in conjunction with the low frequency noise of the surface channel source-follower MOSFET. This effect can be eliminated by using a larger gate surface channel device. This would effectively reduce the source-follower output noise to a level well below the noise of the first two stages so that the source-follower noise will be negligible even in the "roll-off band" of the preamplifier.

3. Dynamic Range and Linearity

The MOSFET preamplifier dynamic range was measured using the wave analyzer and tracking generator as shown in Figure 30. Maximum input signal

**Wave Analyzer
Tracking Generator**

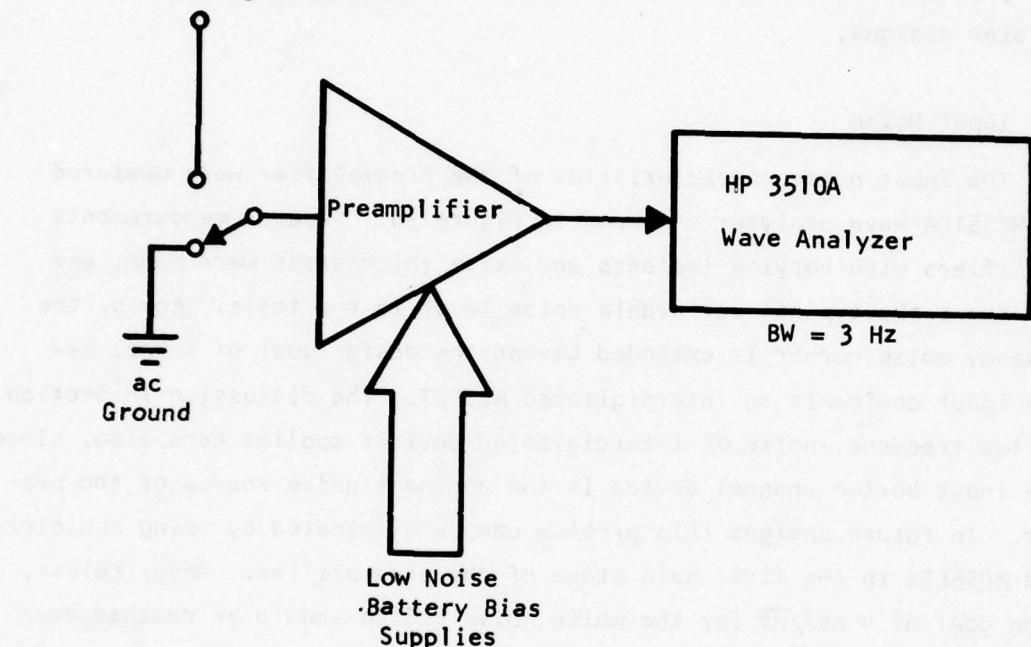


Figure 30. Noise Measurement Set-Up

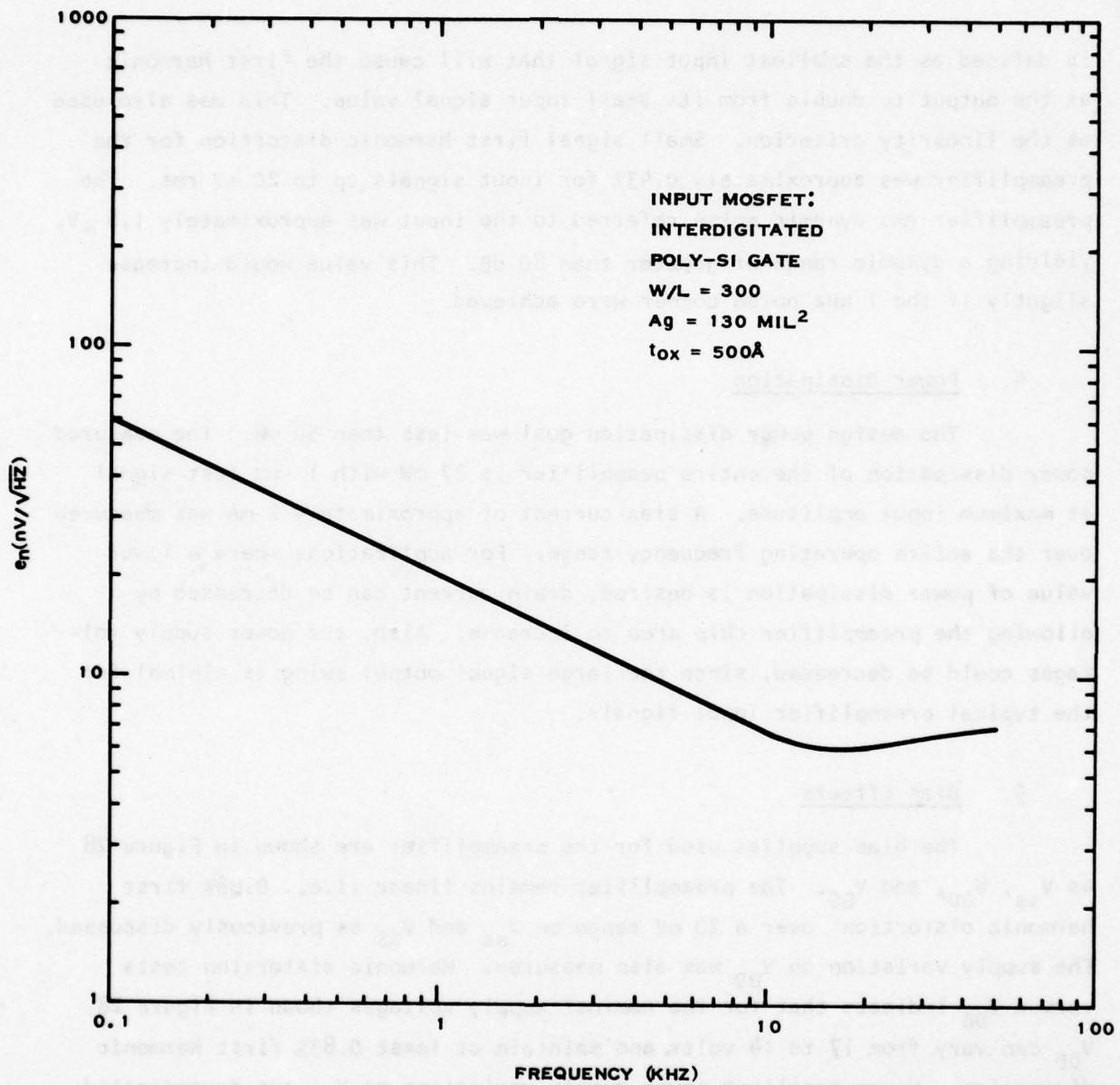


Figure 31. Buried Channel MOS Preamplifier Noise Characteristic

is defined as the smallest input signal that will cause the first harmonic at the output to double from its small input signal value. This was also used as the linearity criterion. Small signal first harmonic distortion for the preamplifier was approximately 0.43% for input signals up to 20 mV rms. The preamplifier rms dynamic noise referred to the input was approximately 1.8 μ V, yielding a dynamic range of greater than 80 dB. This value would increase slightly if the 1 kHz noise corner were achieved.

4. Power Dissipation

The design power dissipation goal was less than 50 mW. The measured power dissipation of the entire preamplifier is 27 mW with 1 kHz test signal at maximum input amplitude. A bias current of approximately 2 mA was measured over the entire operating frequency range. For applications where a lower value of power dissipation is desired, drain current can be decreased by allowing the preamplifier chip area to increase. Also, the power supply voltages could be decreased, since the large signal output swing is minimal for the typical preamplifier input signals.

5. Bias Effects

The bias supplies used for the preamplifier are shown in Figure 28 as V_{ss} , V_{DD} , and V_{GS} . The preamplifier remains linear (i.e., 0.86% first harmonic distortion) over a 20 mV range on V_{ss} and V_{GS} as previously discussed. The supply variation on V_{DD} was also measured. Harmonic distortion tests versus V_{DD} indicate that for the nominal supply voltages shown in Figure 28, V_{DD} can vary from 17 to 14 volts and maintain at least 0.83% first harmonic distortion. Hence excellent power supply variations on V_{DD} are demonstrated. The substrate voltage is -5.0 volt for the present design.

6. Temperature Effects

As shown in Section III.C, MOSFET noise performance is relatively constant over the -50°C to 70°C range. Since the low frequency noise performance

of the preamplifier is dominated by the input MOSFET noise characteristic, the same temperature dependence exists for the preamplifier noise as that shown in Figure 18 for the buried channel MOSFET. Temperature effects of other important preamplifier performance parameters were also determined. The variation of preamplifier gain over the -50°C to 70°C range was slightly more than 1 dB, while the power dissipation decrease from 37.5 mW at -50°C to 25 mW at +70°C was due to a decrease in g_m at lower temperatures.

C. Summary of Preamplifier Test Results

Table 4 summarizes the preamplifier performance characteristics at ambient temperature. The preamplifier gain/bandwidth characteristics were in agreement with design goals, as were dynamic range, linearity, and power dissipation. The primary discrepancy was in the noise characteristics. The higher than expected noise corner is due to the interdigitated design of the input buried channel MOSFET and would be remedied in future designs by using linear in-line or serpentine channels. The increase in white noise at the high frequency end of the preamplifier passband would be eliminated by a larger gate area source-follower MOSFET. The chip area of the preamplifier was less than the design goal.

TABLE 4
PREAMPLIFIER PERFORMANCE CHARACTERISTICS
AT AMBIENT TEMPERATURE

| | <u>Design Goal</u> | <u>Performance</u> |
|-----------------------------------|---|--|
| Gain | 37.5 dB | 37.2 dB |
| Bandwidth | 70 kHz | 60 kHz |
| Input Referred White Noise | 4 nV/Hz | 6 nV/Hz |
| 1/f Corner | 1 kHz | 10 kHz |
| Dynamic Range | 60 dB | 80 dB |
| Power Dissipation | 40 mW | 27 mW |
| Linearity | 1.0% | 0.43% |
| Chip Area | 25.4 mm^2 (1000 mil ²) | 20.3 mm^2 (800 mil ²) |

SECTION V CONCLUSIONS

Under Contract No. F33615-76-C-1221, efforts were directed toward the development of an integrated buried channel MOSFET preamplifier technology designed for low noise performance and possible integration onto a CCD image buffer chip for applications related to forward-looking infrared systems. Extensive experimental evaluation of the noise characteristics of buried channel MOSFETs was accomplished, and the following low noise MOSFET design and process guidelines were established:

- (1) A thin gate oxide may be used to enhance noise performance in both white and low frequency buried channel noise regions of the spectrum.
- (2) MOSFET gate area may be increased to reduce noise levels in the low frequency region.
- (3) A deep buried channel implant results in improved low frequency noise performance at the sacrifice of white noise level.
- (4) Fabricating the buried channel MOSFET with a polysilicon gate material rather than metal enhances low frequency noise performance.
- (5) Buried channel MOSFETs follow the same theory as surface channel in terms of dependence on W/L ratio and bias current with respect to noise performance.
- (6) Interdigitated structure has nearly an order of magnitude higher corner frequency than the in-line structure.

A low noise buried channel preamplifier was designed using the above results for low noise performance. Evaluations of the preamplifiers indicate design goals were met, with the exception of noise levels in both the low frequency and the white regions, which were higher than expected. The MOSFET preamplifier had a nominal gain of 37 dB with a bandwidth of 60 kHz. The dynamic range was approximately 80 dB, and power dissipation was less than 30 mW. The higher-than-expected low frequency noise is due to the buried

channel MOSFET with the interdigitated gate structure. The increase in white noise at the high end of the passband is caused by the low-frequency noise of the surface channel source-follower MOSFET. In subsequent designs, these noise problems can easily be eliminated and desired design goals can be obtained.

In conclusion, the buried channel MOS preamplifier technology has been advanced to the point that this amplifier interface circuitry for possible integration on the CCD image buffer array appears to be feasible.

APPENDIX A
LINEAR INTEGRATED RESISTOR

Linearity (constant resistance) problems are encountered with conventional MOSFET active load elements when used in applications where an ac signal drop across the resistance is large enough to change the bias characteristics of the MOSFET device. A novel design approach to a linear MOS resistive element developed under this program is discussed in this appendix.

For a standard implanted resistor as used in the buried channel CCD process, the I-V curves resemble those shown in Figure A-1. Structurally, this device is a buried channel MOSFET without a gate; i.e., there is no metal (or polysilicon) over the channel area. Therefore, the surface over the channel, the effective MOSFET gate area, is electrically uncontrolled. This implies the V_{GS} is floating, and the slope of the curve can change from resistor to resistor, depending on the state of the pseudogate, that is, exposed gate oxide (Figure A-2).

Putting a gate over the channel would solve the above problem. However, the device would no longer be an implanted resistor, but a MOSFET being used as an active load. To use a MOSFET as an active load or a resistor as in the feedback network of an amplifier, the gate must be tied back to the drain or source when buried channel MOSFETs are used. The arrangements are shown in Figure A-4. The I-V curves for configuration 4(b) are similar to those of the implanted resistor in Figure A-1. However, the gate voltage is now controlled, and the device can be operated at a constant V_{GS} of 0 V. It should be noted in Figure A-1 that the curves are slightly nonlinear over a range of V_{DS} . When used as a resistor as in Figure A-3 for R_F , V_{DS} changing can cause the effective resistance to change. Therefore, Figure A-4(b) does not provide a complete solution to the problem. In Figure A-4(a) the gate is tied back to the drain so that the MOSFET operates along the constant $V_{GS} = V_{DS}$ curves shown in Figure A-5. It can also be seen that the curves are slightly nonlinear for a wide range of V_{DS} . Again, the resistor configuration of Figure

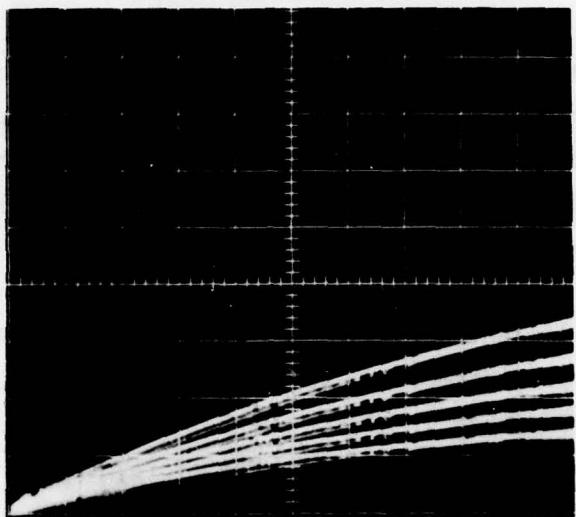


Figure A-1. Implanted Resistor Curves and MOSFET Curves for Figure A-4(b) Circuit

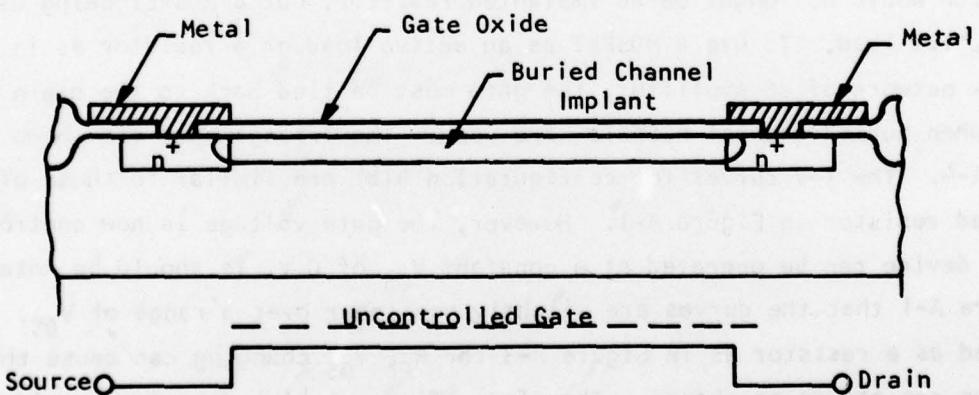


Figure A-2. Implanted Resistor

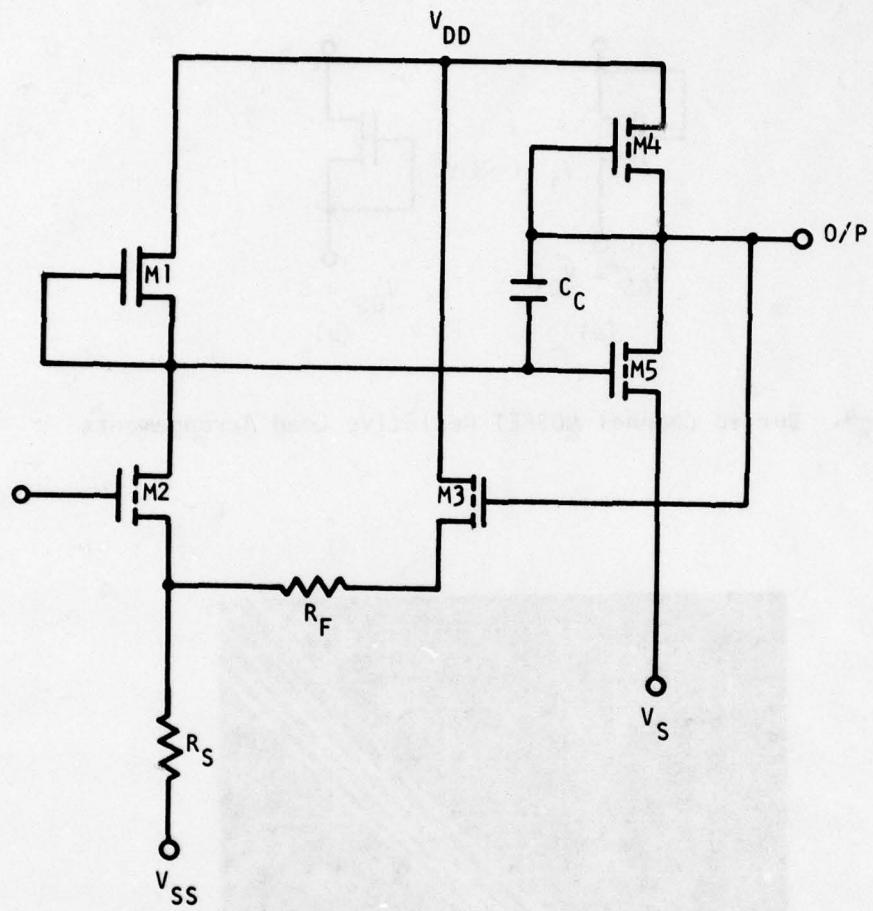


Figure A-3. Feedback Amplifier

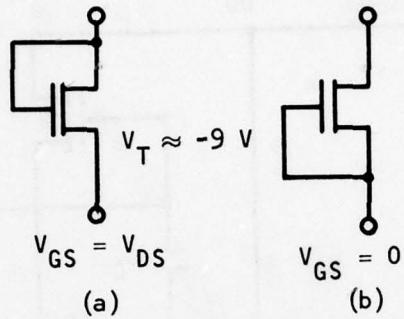


Figure A-4. Buried Channel MOSFET Resistive Load Arrangements

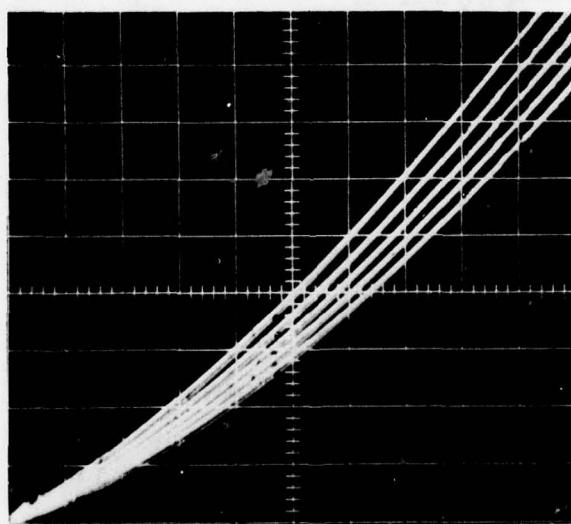


Figure A-5. I-V Curves Corresponding to Figure A-4(a) Circuit

A-4(a) is not a complete solution. If we compare the behavior of devices A-4(b) and A-4(a) by referring to the respective I-V curves, Figures A-1 and A-5, it can be seen that the curves of A-4(b) have negative second derivatives with respect to V_{DS} , while the curves of A-4(a) have a positive second derivative. It seems possible to combine the two effects such that they tend to offset one another, yielding a more linear, more "resistor-like" I-V curve. A technique for implementing this behavior is shown in Figure A-6, and the I-V curves for this configuration are shown in Figure A-7. As can be seen in Figure A-7, the I-V curves are quite linear over a 10 V range for V_{DS} for a constant V_{GS} . The sizes of M1 and M2 are designed with W/L ratios such that the resultant I-V curve is linear (see Figure A-8).

The principal area of application of this linear resistor technique would be for implementing the series element in the feedback network of an amplifier (such as R_F in Figure A-3). R_F is usually a large device in terms of required resistance; therefore, the voltage across this element varies with the output signal, and V_{DS} changes considerably. This is true for amplifiers that have a large gain. For a small gain amplifier or an amplifier that has a small output signal with respect to dc bias voltages the problem is not as pronounced, since the change in V_{DS} is also very small.

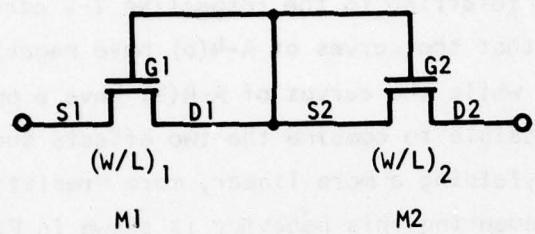


Figure A-6. MOSFET I-V Linearizing Technique for Implementing Integrated Resistors

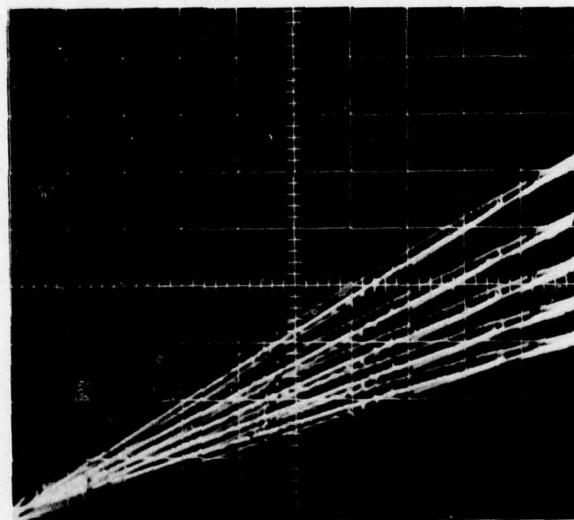


Figure A-7. Curves for Circuit in Figure A-6

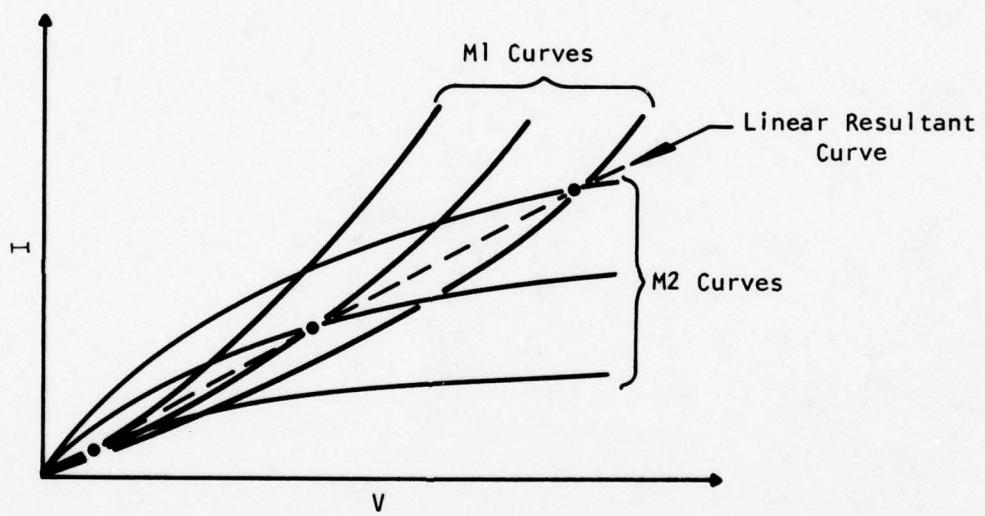


Figure A-8. Superposition of Figures A-1 and A-5 to Yield A-8
Linear Characteristic of Figure A-7

APPENDIX B
TEST FIXTURE

The block diagram of the test fixture used in evaluating the test MOSFETs and preamplifiers in terms of gain performance as well as noise characteristics is shown in Figure B-1, while Figure B-2 shows a detailed schematic of this test box. The photograph of the test fixture and measuring equipment is shown in Figure B-3. The ac gain measurements were made in the same box as noise measurements. When noise data were being taken, the gate of the MOSFET was ac-grounded via a switch in the test box. The components within the test box circuit such as low noise film resistors were carefully selected to have low noise characteristics.

Measurements were made in a shielded room environment. Sample measurements of known reference were repeated at various intervals to insure that there was no contamination from surrounding electromagnetic activity. The measurements were made with a wave analyzer that had sufficient sensitivity to allow direct measurement of the test MOSFET in a low gain configuration without adding any amplification between the test MOSFET and the wave analyzer input. Particular attention was given to filtering dc power supplies to insure no contamination of the data due to noisy power supplies.

The photomicrograph of the buried channel MOSFET preamplifier test bar is shown in Figure B-4. This bar contains a number of test MOSFET structures that have a variety of geometric configurations in terms of W/L ratio, gate area, gate topology, and gate material. The W/L ratio is varied from 0.5 to 350 while the gate area ranges from 0.5 mm^2 to 3.2 mm^2 (6 mil^2 to 130 mil^2). As shown in this figure, both in-line and large interdigitated structures are used. Both polysilicon and aluminum gate materials are used in several devices that have all other geometric parameters remaining the same. Several buried channel MOS preamplifier circuits are shown. The schematic for this buried channel low noise MOS preamplifier is shown in Figure 27. The configuration as shown in the photomicrograph of the test bar allows the experimental testing of different stages in the basic preamplifier structure. A number of test structures for process monitoring are also shown in Figure B-4.

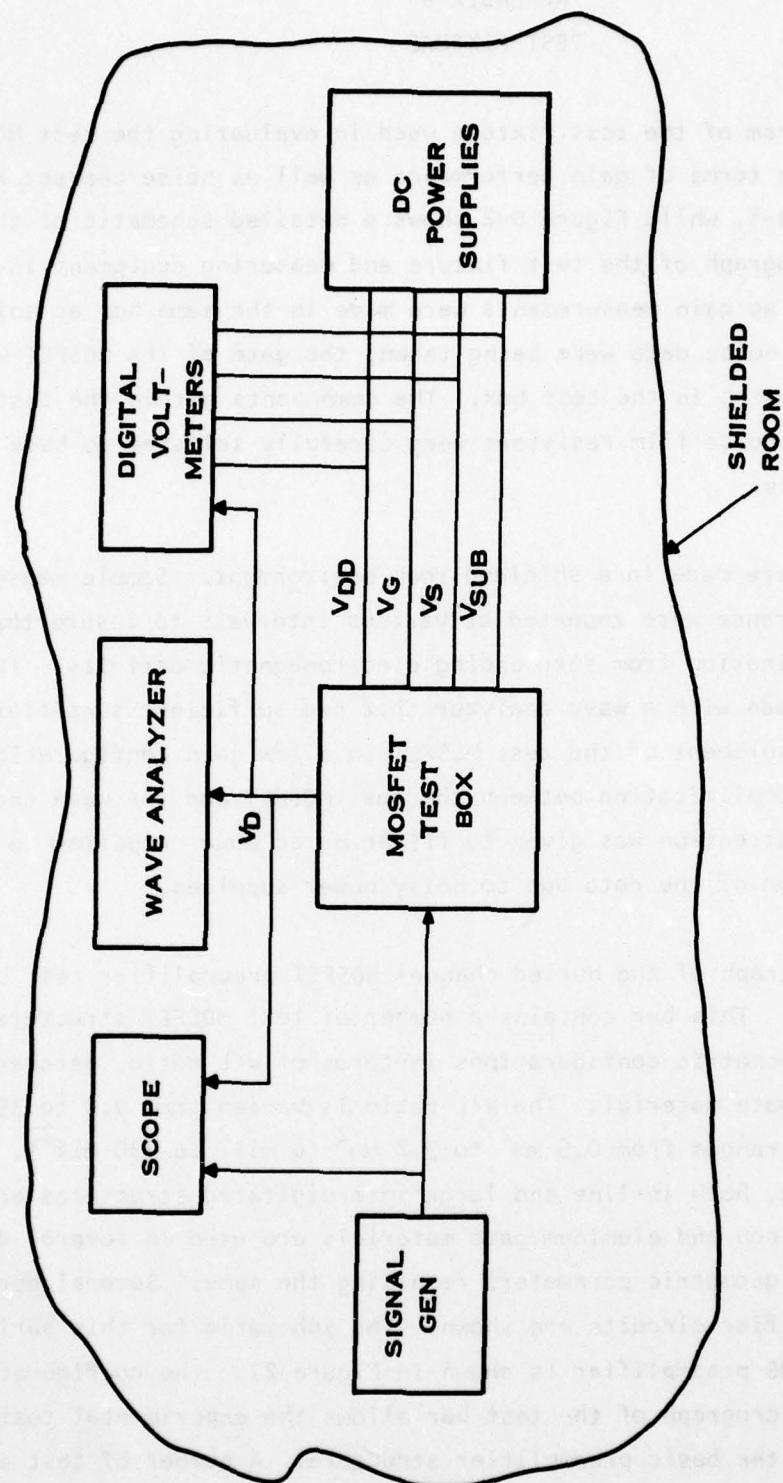


Figure B-1. Noise Measurement Test Station

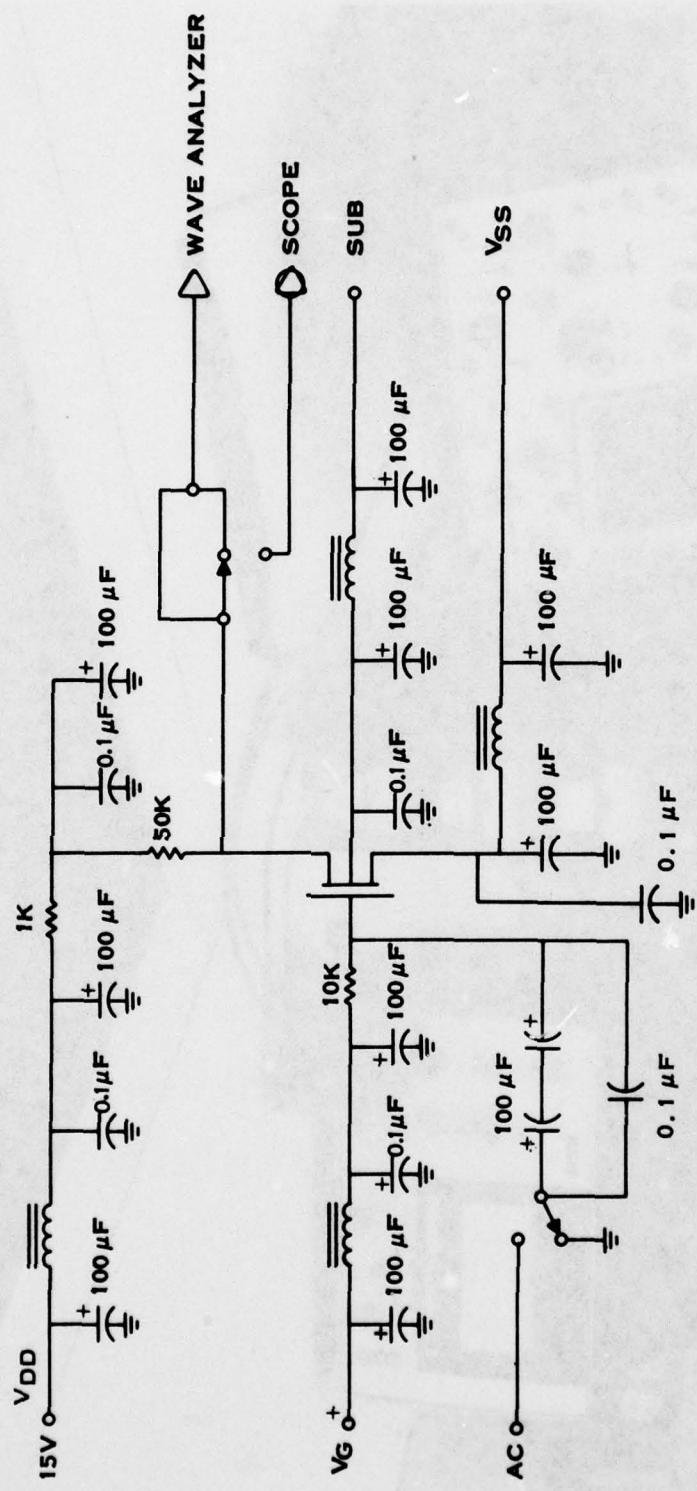


Figure B-2. MOSFET Noise Test Box

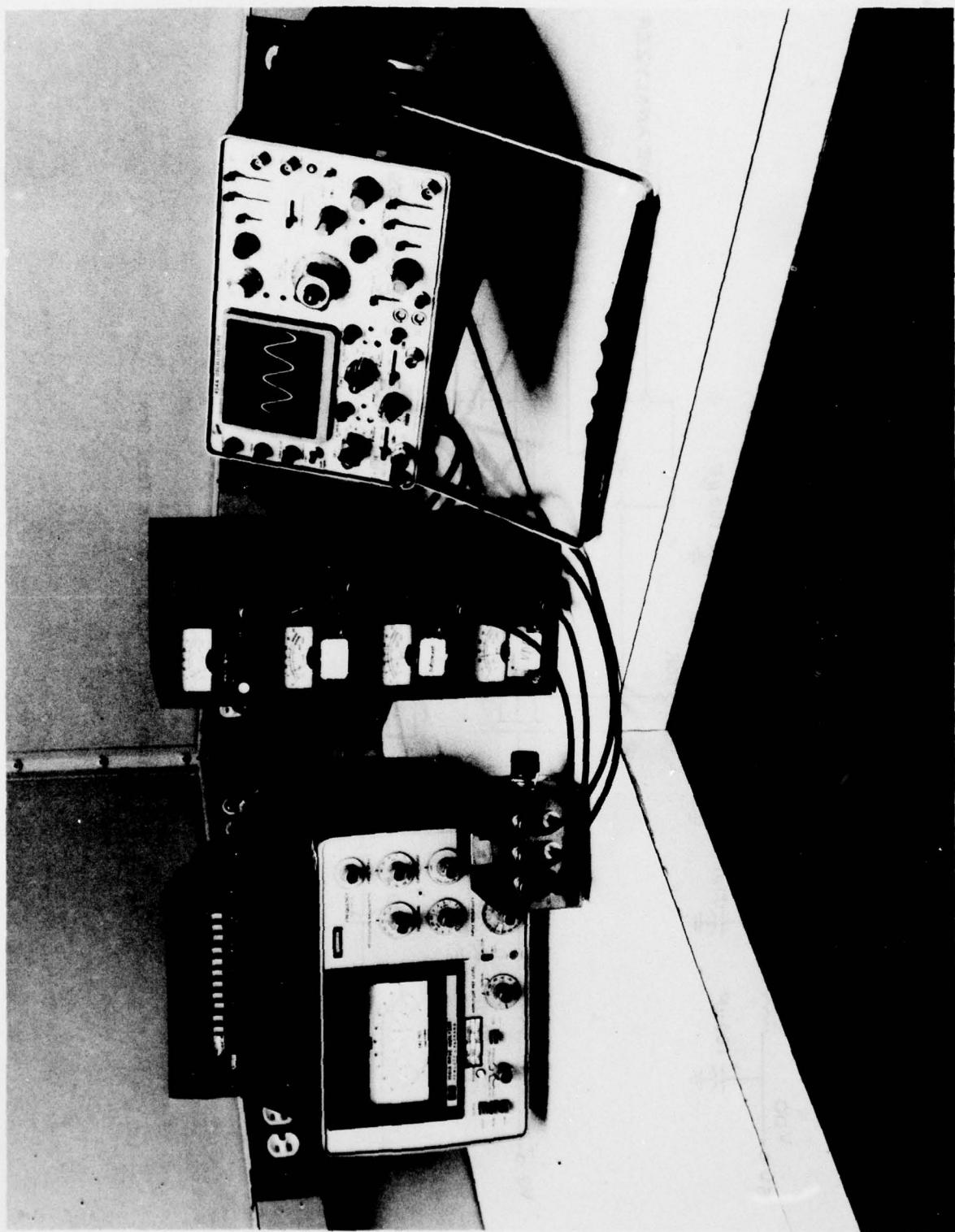


Figure B-3. Photograph of Low Noise Test Fixture and Measuring Equipment

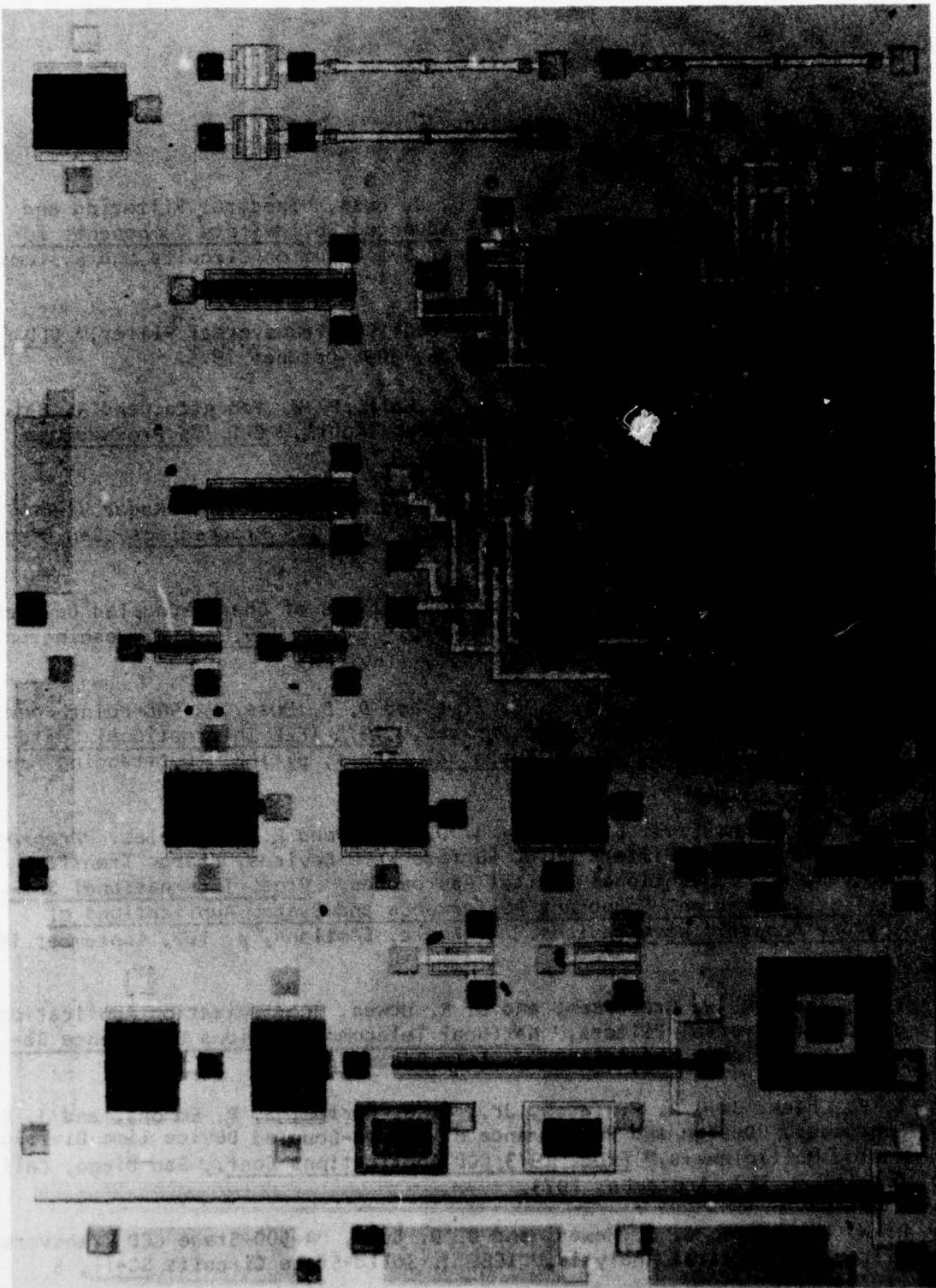


Figure B-4. Photomicrograph of the Low Noise Buried Channel MOSFET Preamplifier test bar

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